ISCAS 2004 Forum:
New Era of Technology

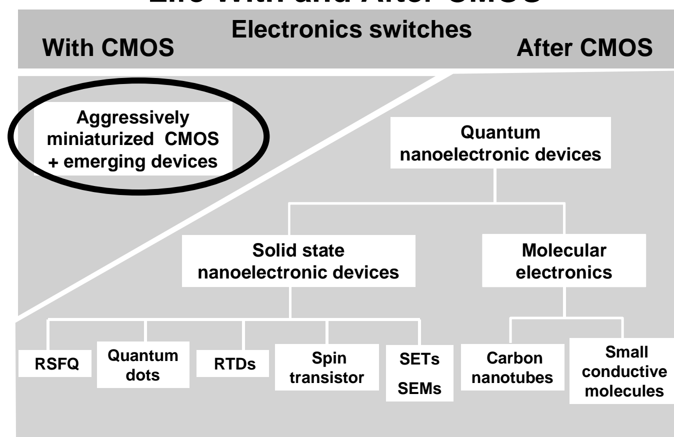
Design Challenges for Nanoelectronic Circuits and Systems

Yusuf Leblebici

Microelectronic Systems Laboratory
Swiss Federal Institute of Technology
Lausanne – Switzerland

23 May 2004

Life With and After CMOS

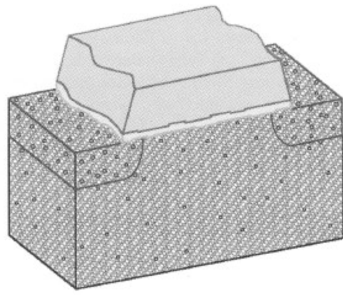


After A. M. Ionescu, M. J. Declercq, S. Mahapatra, K. Banerjee, J. Gautier, "Few Electron Devices: Toward Hybrid CMOS-SET Integrated Circuits," DAC 2002, June 2002, pp. 88-93.

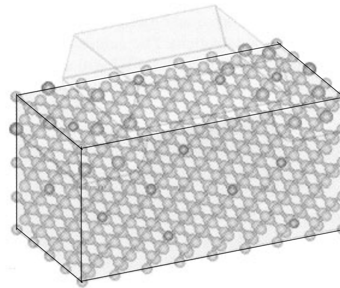
IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 50, NO. 9, SEPTEMBER 2003 1837

Simulation of Intrinsic Parameter Fluctuations in Decananometer and Nanometer-Scale MOSFETs

Asen Asenov, *Member, IEEE* , Andrew R. Brown, John H. Davies, Savas Kaya, and Gabriela Slavcheva



20 nm MOSFET (2010 ?)
50 Si atoms along the channel



4 nm MOSFET (2020 ?)
10 Si atoms along the channel

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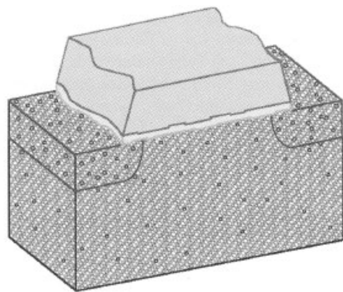
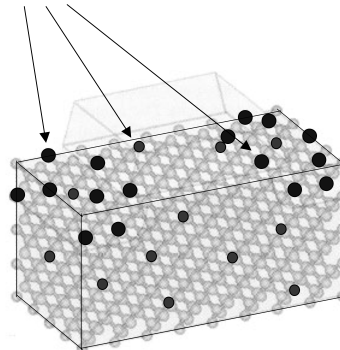
Strongly Irregular Device Behavior Expected !



20 nm MOSFET (2010 ?)
50 Si atoms along the channel



4 nm MOSFET (2020 ?)
10 Si atoms along the channel

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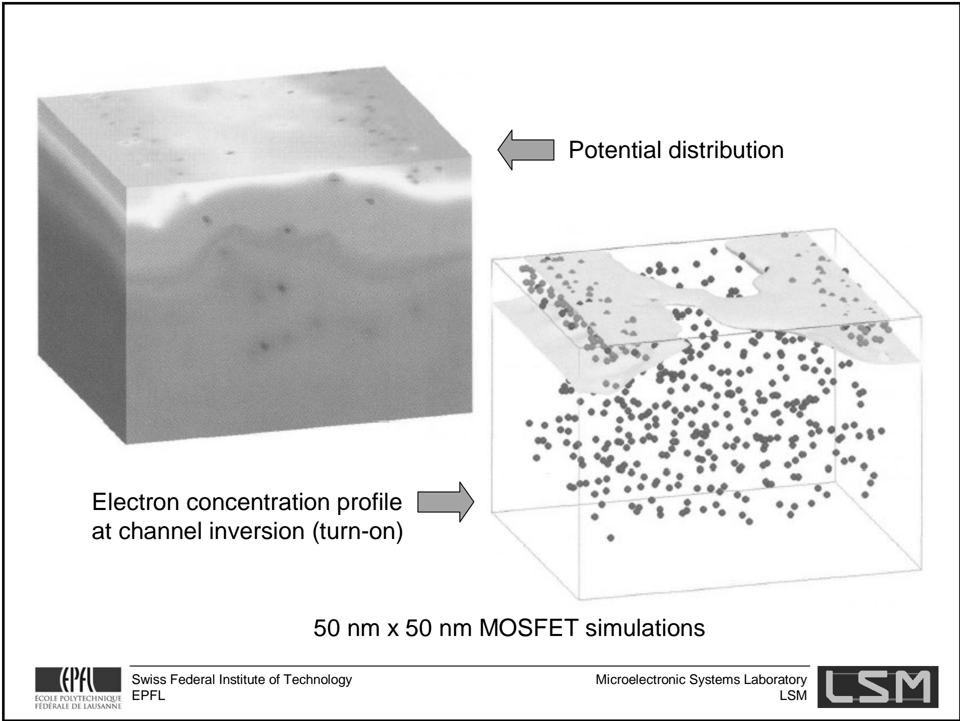
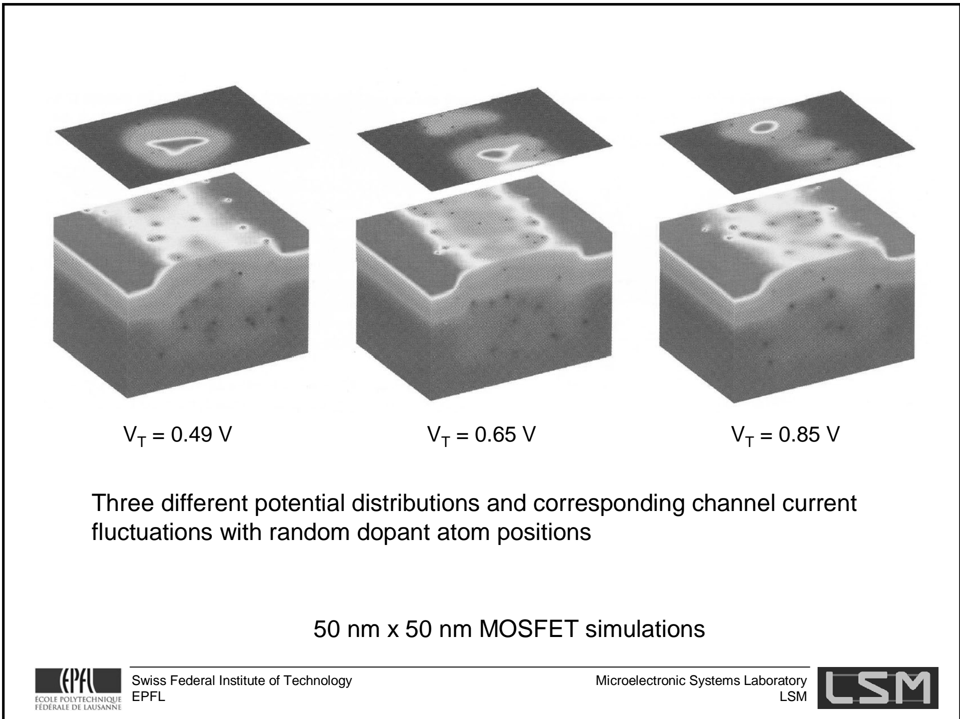

Potential distribution
Electron concentration profile
at channel inversion (turn-on)
50 nm x 50 nm MOSFET simulations
Swiss Federal Institute of Technology
EPFL
Microelectronic Systems Laboratory
LSM


V_T = 0.49 V
V_T = 0.65 V
V_T = 0.85 V
Three different potential distributions and corresponding channel current fluctuations with random dopant atom positions
50 nm x 50 nm MOSFET simulations
Swiss Federal Institute of Technology
EPFL
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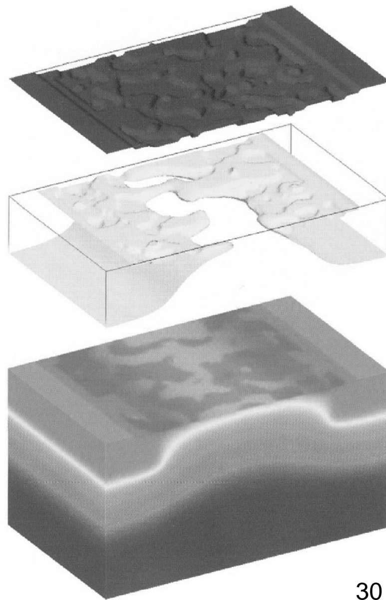


Potential distribution and electron concentration profile at channel inversion (turn-on)

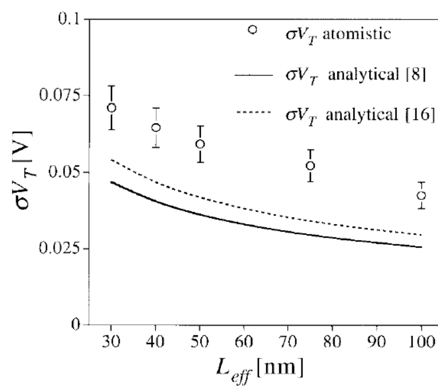
30 nm x 30 nm MOSFET simulations

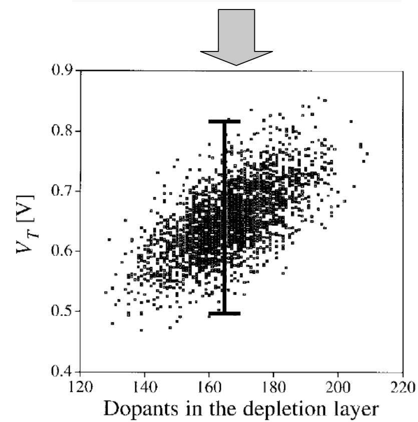
IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 45, NO. 12, DECEMBER 1998 2505

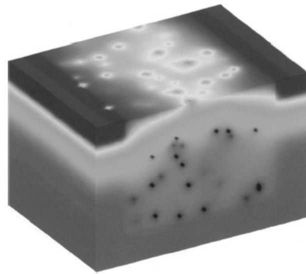
Random Dopant Induced Threshold Voltage Lowering and Fluctuations in Sub-0.1 μm MOSFET's: A 3-D "Atomistic" Simulation Study

Asen Asenov

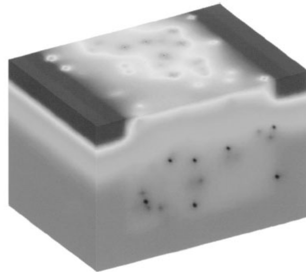
Dramatic fluctuation of the threshold voltage even with the <u>same</u> number of dopant atoms !







(a)



(b)

Potential distribution with 170 random dopant atoms in the channel region.

(a) Threshold voltage 0.78 V

(b) Threshold voltage 0.56 V

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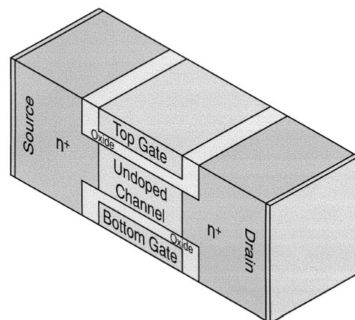
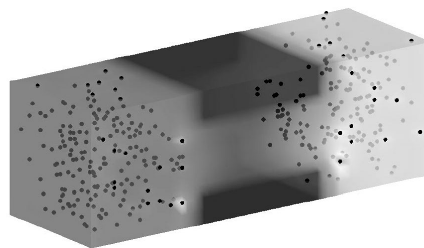
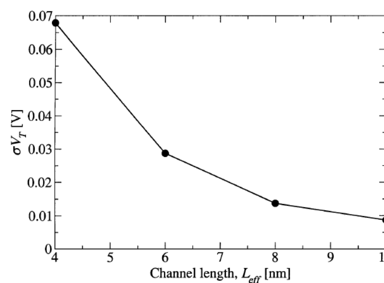


Schematic illustration of the simulated double-gate MOSFETs.





Similar levels of uncertainty expected for new double-gate MOSFET structures as well.

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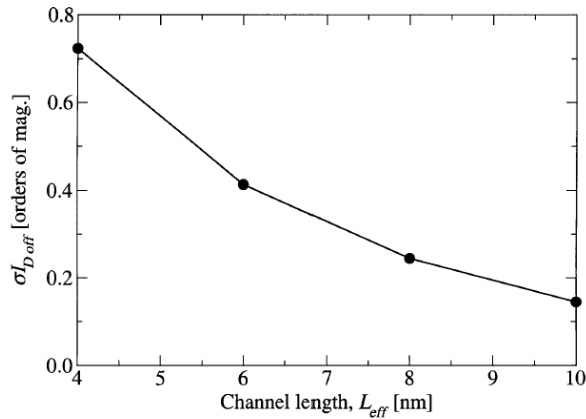
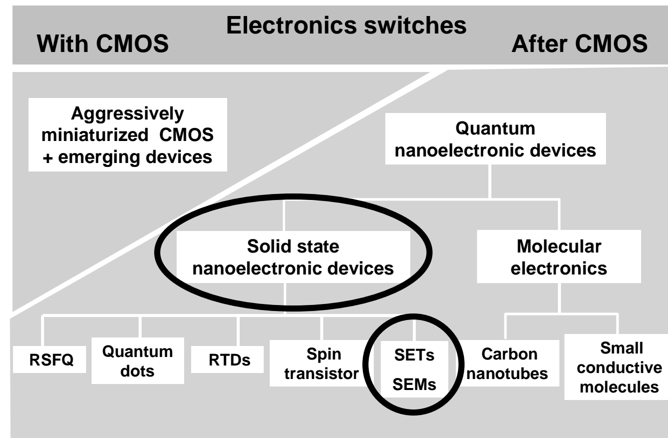


Standard deviation of MOSFET off-current approaching one order of magnitude !

Logic circuit design with such unpredictable device characteristics may result in multiple “stuck-open” or “stuck-short” faults.

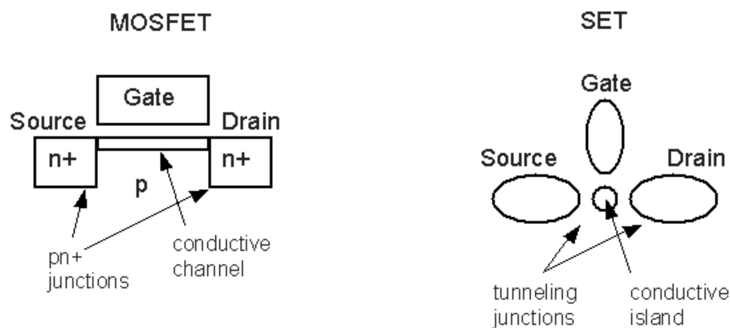
How to design reliable systems with inherently unreliable components ?

Life With and After CMOS

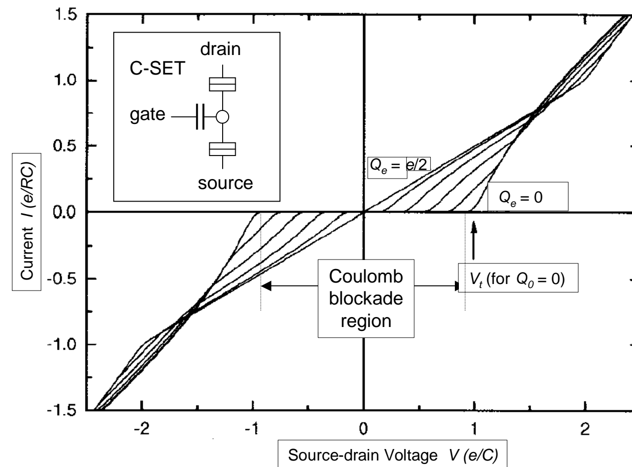


After A. M. Ionescu, M. J. Declercq, S. Mahapatra, K. Banerjee, J. Gautier, "Few Electron Devices: Toward Hybrid CMOS-SET Integrated Circuits," DAC 2002, June 2002, pp. 88-93.

Comparison of Nanometer-Scale MOSFET and SET

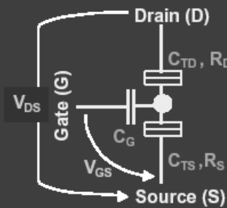


Single-Electron Transistor (SET) Characteristics



Typical current-voltage characteristics of an C-SET (after K. Likharev)

Introduction: SET Preliminaries



C_{TD}: **Drain tunnel junction capacitance**

C_{TS}: **Source tunnel junction capacitance**

R_D : **Drain tunnel junction resistance**

R_S : **Source tunnel junction resistance**

C_G : **Gate capacitance**

$$C_\Sigma = C_G + C_{TD} + C_{TS}$$

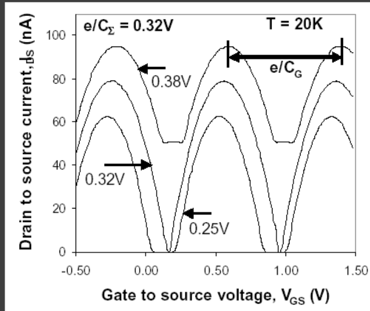
To obtain "Coulomb Blockade Effect" one needs:

- **opaque tunnel junctions: $R_T > R_Q$~26kΩ**
- **$(e^2/C_\Sigma):k_BT > 10 \sim 40$, therefore, needs very tiny island diameter for room temperature operation (~ 1nm)**

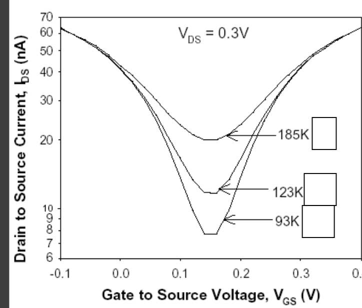
After Mahapatra et al., IEDM 2003

Introduction: SET Characteristics

I_{DS} vs. V_{GS} @ $\#V_{DS}$



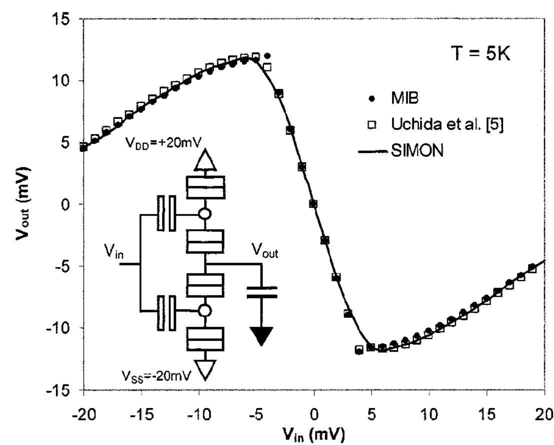
I_{DS} vs. V_{GS} @ $\#T$



$C_{TD} = C_{TS} = 0.15aF$, $C_G = 0.2aF$, $R_{TD} = R_{TS} = 1M\Omega$

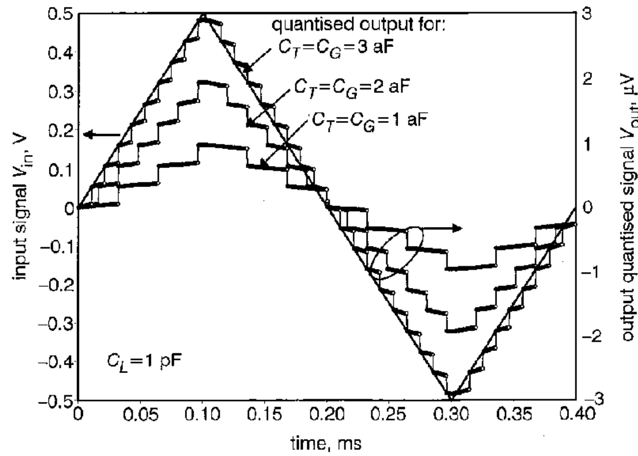
After Mahapatra et al., IEDM 2003

SET Circuit Examples



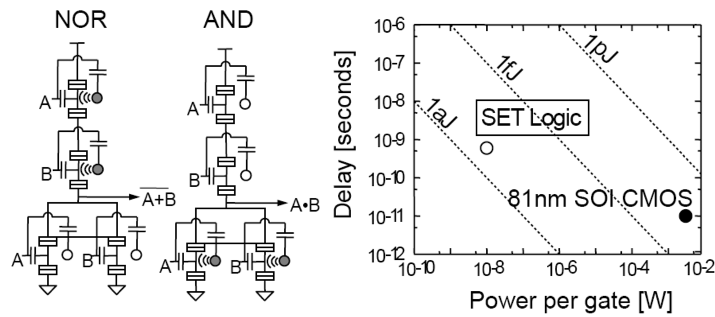
Input-output characteristics of an SET-based inverter circuit

SET Circuit Examples



Simulated operation of an SET-based quantizer circuit

Power Estimation



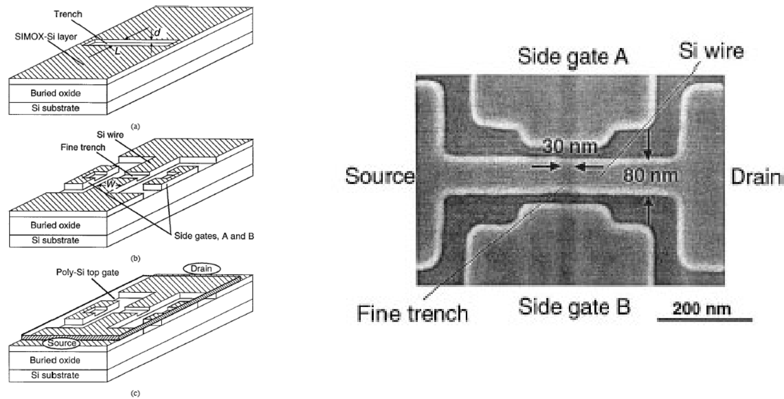
Good candidate for replacing Si CMOS technology ?
… or <u>co-existing with</u> Si CMOS technology ?

After Uchida et al., ISSCC 2002

IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 47, NO. 1, JANUARY 2000 147

Fabrication Method for IC-Oriented Si Single-Electron Transistors

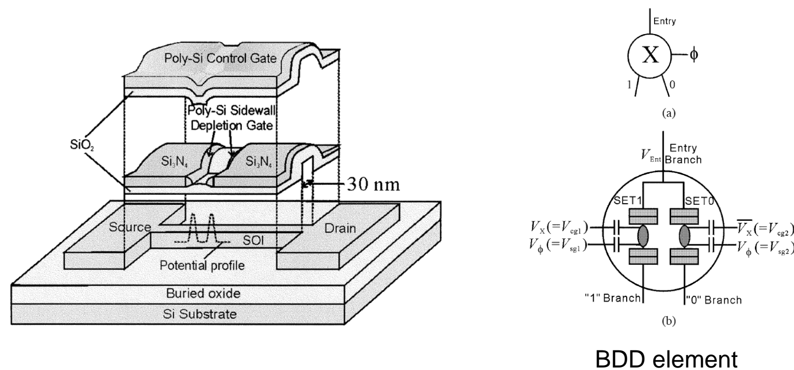
Yukinori Ono, Yasuo Takahashi, Kenji Yamazaki, Masao Nagase, Hideo Namatsu, Kenji Kurihara, and Katsumi Murase



170 IEEE TRANSACTIONS ON NANOTECHNOLOGY, VOL. 1, NO. 4, DECEMBER 2002

Single-Electron Transistors Based on Gate-Induced Si Island for Single-Electron Logic Application

Dae Hwan Kim, Suk-Kang Sung, Kyung Rok Kim, Jong Duk Lee, *Member, IEEE*, and Byung-Gook Park, *Member, IEEE*

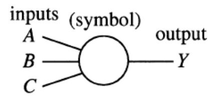


BDD element

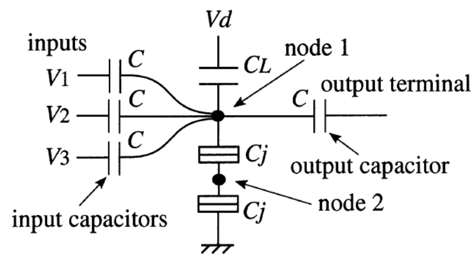
IEEE TRANSACTIONS ON NANOTECHNOLOGY, VOL. 2, NO. 1, MARCH 2003 15

A Majority-Logic Device Using an Irreversible Single-Electron Box

Takahide Oya, Tetsuya Asai, Takashi Fukui, and Yoshihito Amemiya



inputs			output
A	B	C	Y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1



Possible Advantages of SETs

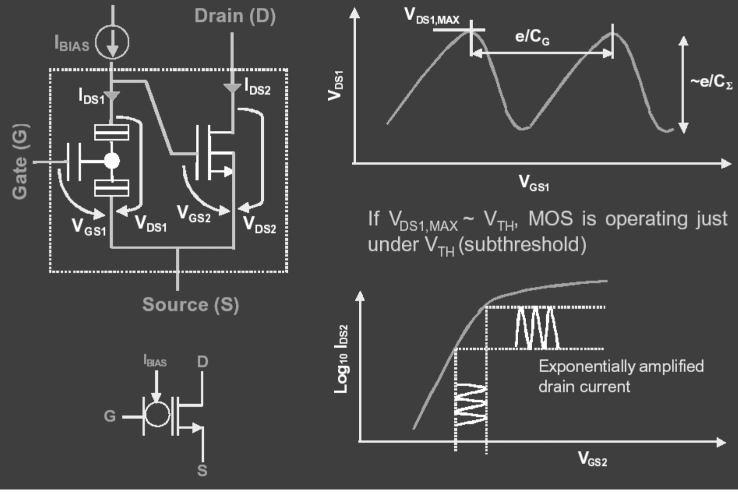
or: How to exploit a new technology ?

- Higher integration density
- Lower power dissipation

} Closer to “classical” design, only better (?)

- New device behavior and functionality } More open-ended

In both cases, successful implementation depends on solving the reliability problem.



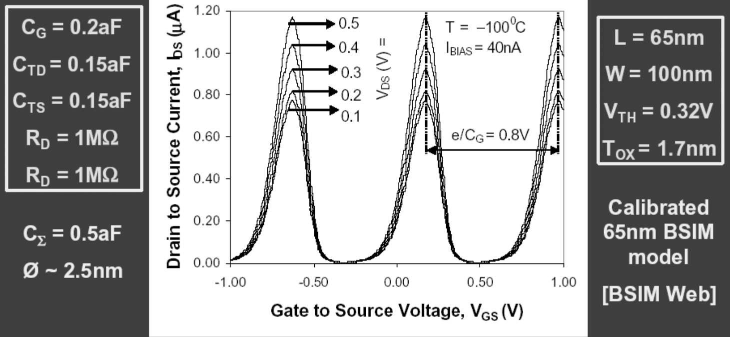
After Mahapatra et al., IEDM 2003

SETMOS Device Characteristics (1)

I_{DS} vs V_{GS} @ #V_{DS}

C_G = 0.2aF
C_{TD} = 0.15aF
C_{TS} = 0.15aF
R_D = 1MΩ
R_D = 1MΩ

C_Σ = 0.5aF
Ø ~ 2.5nm



L = 65nm
W = 100nm
V_{TH} = 0.32V
T_{OX} = 1.7nm

Calibrated 65nm BSIM model
[BSIM Web]

After Mahapatra et al., IEDM 2003

CMOS & SET: Competitor/Collaborator?

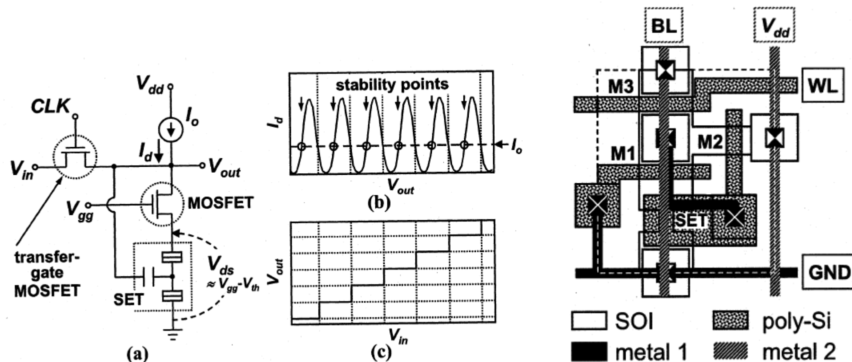
SET	CMOS
+ Nano Scale device + Ultra low power dissipation + New functionalities	+ High Speed + Very Stable Technology
– Technology for room temperature operation – Reproducibility at nanoscale – Low Current drive (~nA) – Back ground charge effect	– SCE/DIBL – Power dissipation – Process variations at nanoscale

After Mahapatra et al., IEDM 2003

462 IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 50, NO. 2, FEBRUARY 2003

A Multiple-Valued Logic and Memory With Combined Single-Electron and Metal–Oxide–Semiconductor Transistors

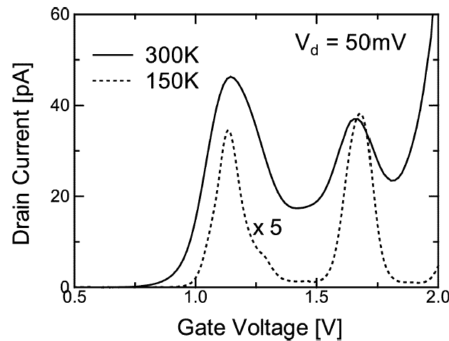
Hiroshi Inokawa, *Member, IEEE*, Akira Fujiwara, *Member, IEEE*, and Yasuo Takahashi, *Member, IEEE*

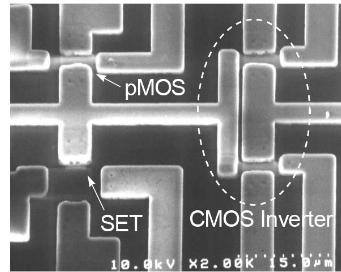


IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 50, NO. 7, JULY 2003 1623

Programmable Single-Electron Transistor Logic for Future Low-Power Intelligent LSI: Proposal and Room-Temperature Operation

Ken Uchida, *Member, IEEE*, Junji Koga, Ryuji Ohba, and Akira Toriumi, *Member, IEEE*





SET/CMOS Hybrid

Why Hybrid?

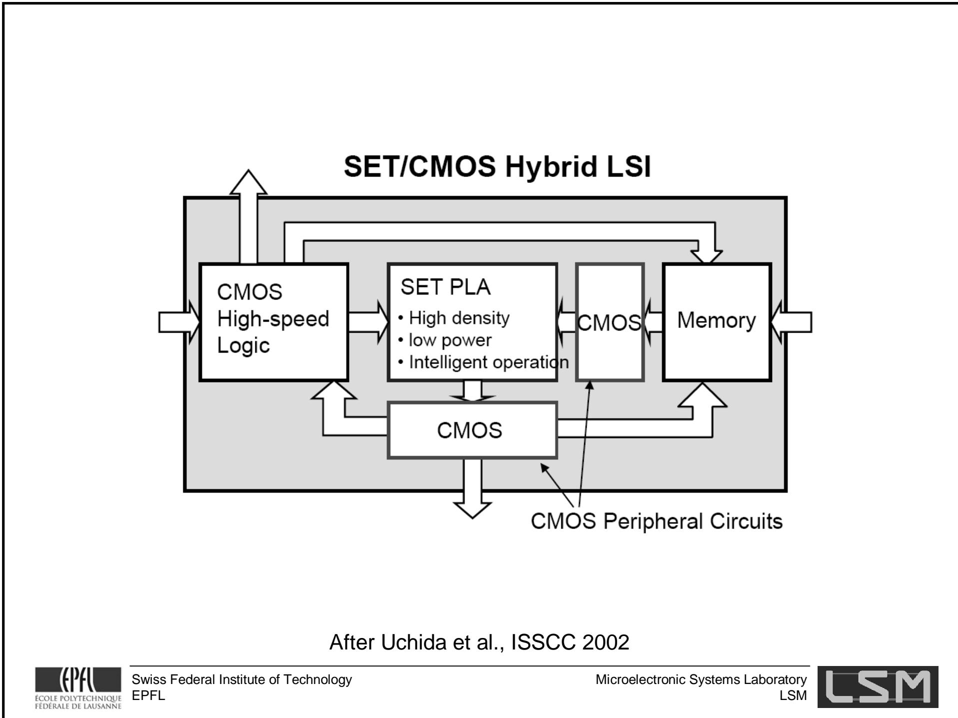
✓ *SETs have the low power-consumption property and high functionality.*

✓ *<u>CMOS advantages</u> compensate for <u>SET disadvantage</u>.*

CMOS advantages	SET disadvantage
• High Input impedance	• High output impedance
• High driving capability	• Low driving capability
• High voltage gain	• Small V_{ds}

Therefore,
SET/CMOS hybrid is expected to be an ultimate LSI.

After Uchida et al., ISSCC 2002


SET/CMOS Hybrid LSI
CMOS
High-speed
Logic
SET PLA
• High density
• low power
• Intelligent operation
CMOS
Memory
CMOS
CMOS Peripheral Circuits
After Uchida et al., ISSCC 2002
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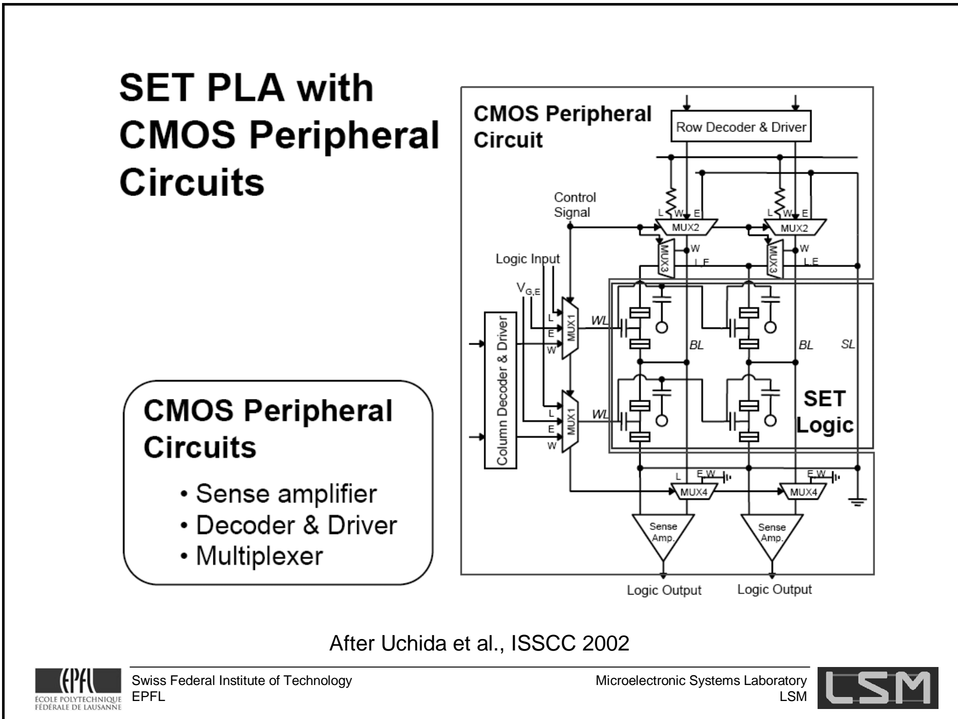
SET PLA with
CMOS Peripheral
Circuits
CMOS Peripheral
Circuit
Row Decoder & Driver
Control
Signal
Logic Input
MUX1
MUX2
MUX3
MUX4
WL
BL
SL
Column Decoder & Driver
SET
Logic
Sense
Amp.
Logic Output
Logic Output
CMOS Peripheral
Circuits
• Sense amplifier
• Decoder & Driver
• Multiplexer
After Uchida et al., ISSCC 2002
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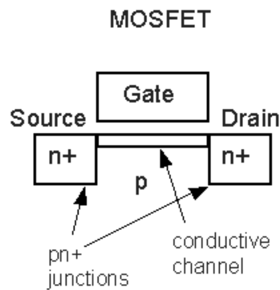
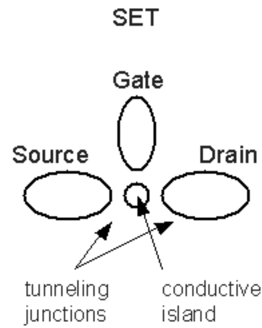
MOSFET and SET Reliability Issues





Short channel effects
Source-to-drain tunneling
Gate oxide leakage
Process variations
Static leakage
Power scaling

Temperature dependence
Background charge
Noise sensitivity
Process variations
Interconnect

Expected device failure rates in the order of 10 - 20 % !!

How to design reliable systems with inherently unreliable components ?

Molecular Electronics: Devices, Systems and Tools for Gigagate, Gigabit Chips

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André DeHon
Dept. of CS, 256-80
California Institute of Technology
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Seth Copen Goldstein
School of Computer Science
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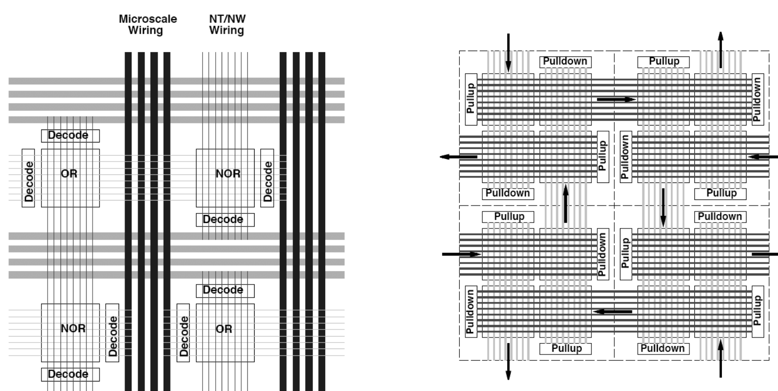
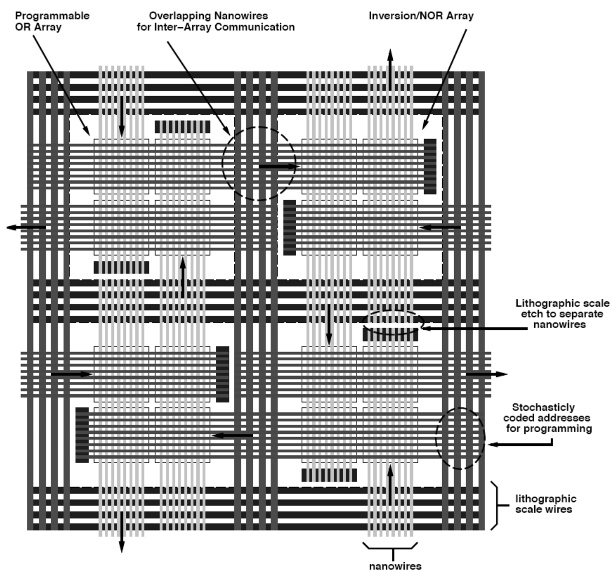
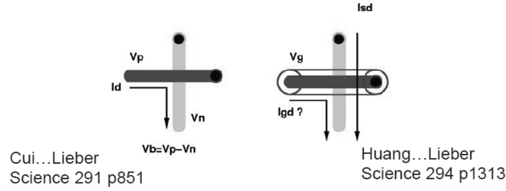
⟨seth@cs.cmu.edu⟩





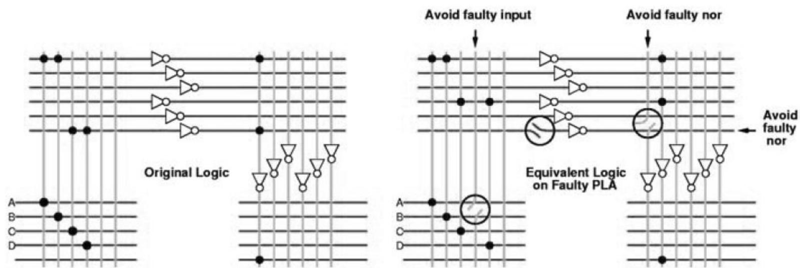
After DeHon et al.

Diode and FET Junctions



Cui…Lieber
Science 291 p851

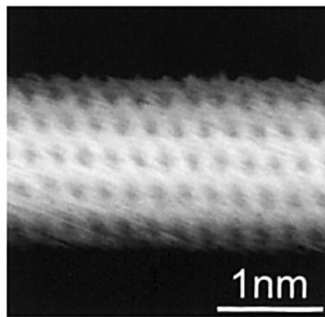
Huang…Lieber
Science 294 p1313

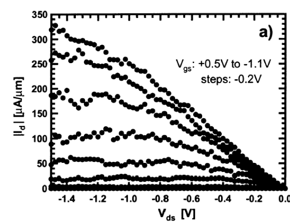


184 IEEE TRANSACTIONS ON NANOTECHNOLOGY, VOL. 1, NO. 4, DECEMBER 2002

Carbon Nanotube Electronics

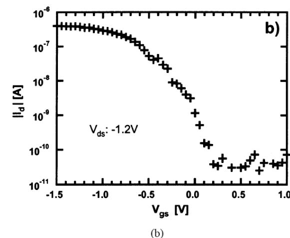
Joerg Appenzeller, *Member, IEEE*, Joachim Knoch, Richard Martel, Vincent Derycke, Shalom J. Wind, *Senior Member, IEEE*, and Phaedon Avouris





(a)

FET



(b)

Diode

Future nano-electronic circuits may also be built using carbon nanotube components !

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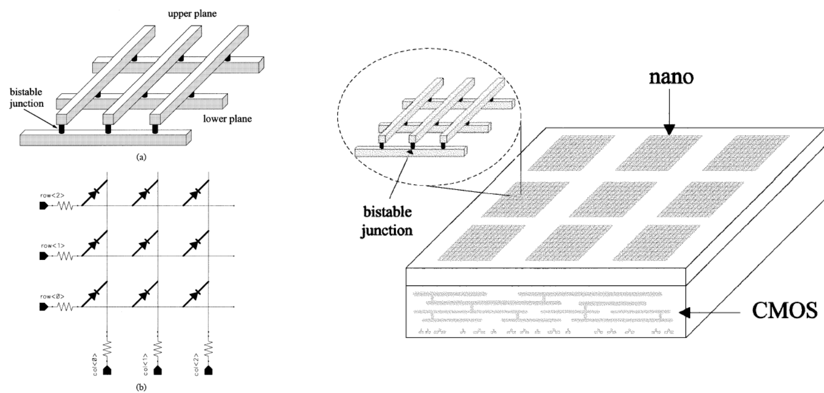
CMOS/Nano Co-Design for Crossbar-Based Molecular Electronic Systems

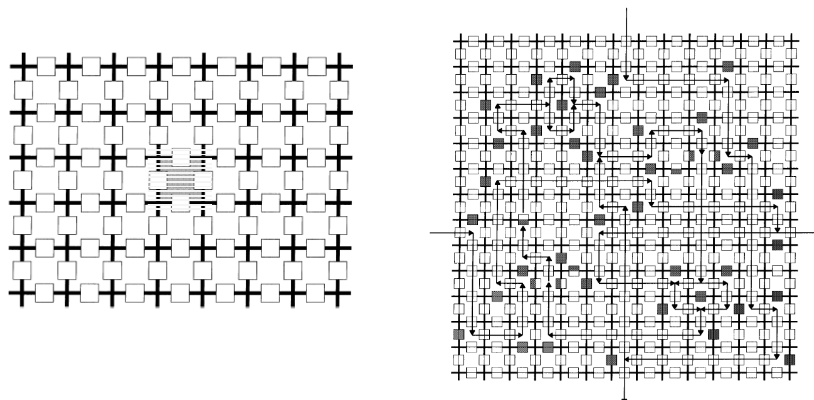
Matthew M. Ziegler, *Student Member, IEEE,* and Mircea R. Stan, *Senior Member, IEEE*

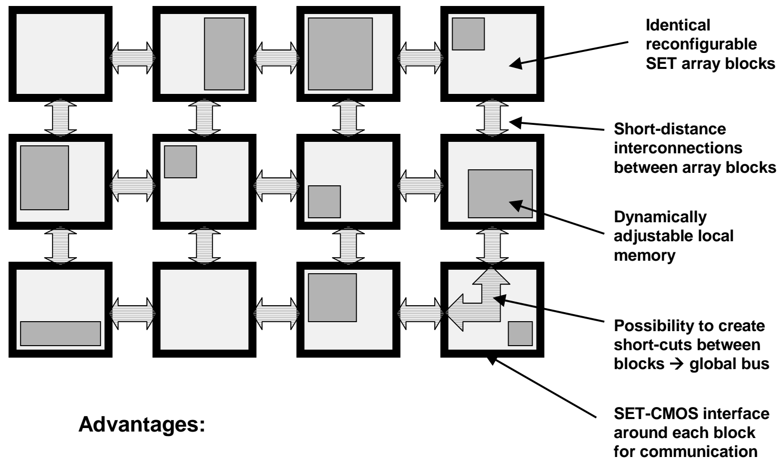


IEEE TRANSACTIONS ON NANOTECHNOLOGY, VOL. 3, NO. 1, MARCH 2004 187

Fault-Tolerance in Nanocomputers: A Cellular Array Approach

Ferdinand Peper, *Member, IEEE*, Jia Lee, Fukutaro Abo, Teijiro Isokawa, *Member, IEEE*, Susumu Adachi, Nobuyuki Matsui, and Shinro Mashiko



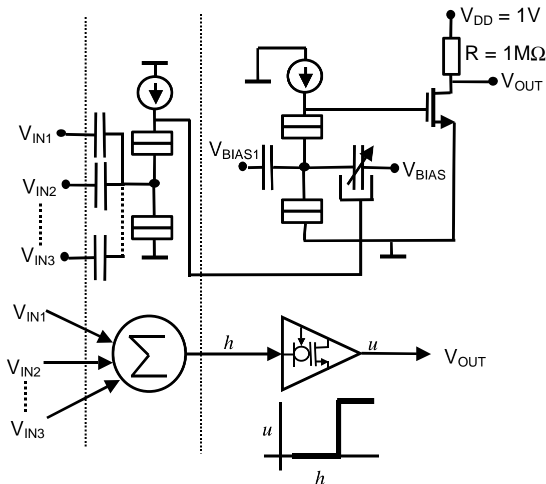


Advantages:

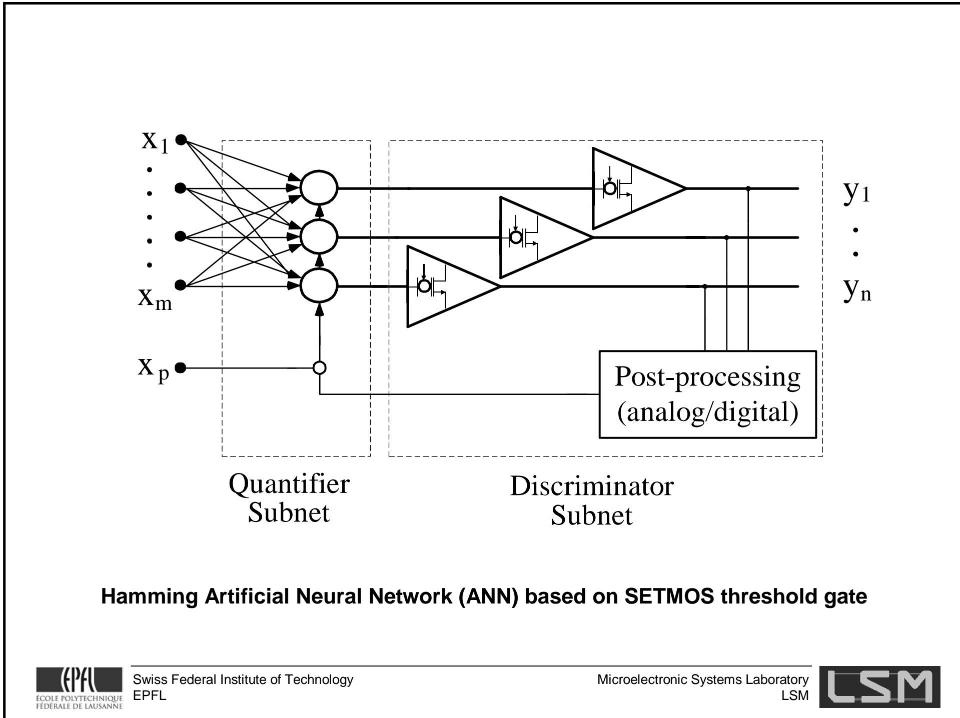
- Very regular fine-grained array architecture
- Array suitable for logic and/or memory
- Fault tolerance at cell level possible
- Dynamic reconfigurability for customization

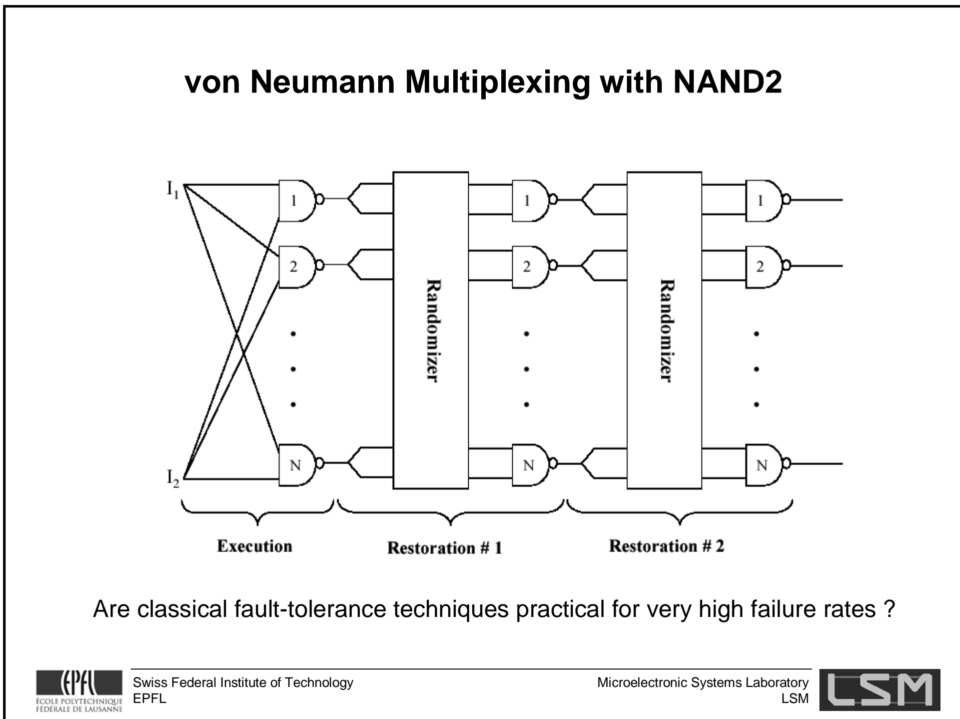
One possibility for robust design:

Adopt neural-network principles to improve immmunity against device failures.

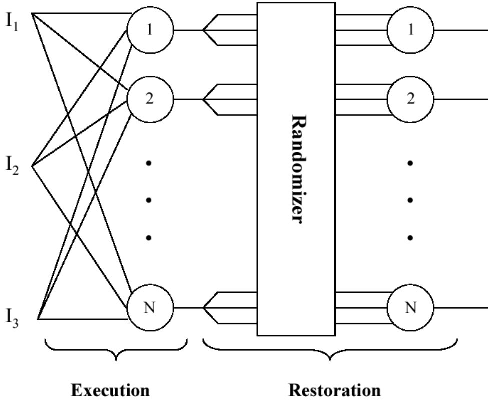


CMOS-SET hybrid neuron cell based on threshold function


x1
xm
xp
y1
yn
Post-processing
(analog/digital)
Quantifier
Subnet
Discriminator
Subnet
Hamming Artificial Neural Network (ANN) based on SETMOS threshold gate
Swiss Federal Institute of Technology
EPFL
Microelectronic Systems Laboratory
LSM

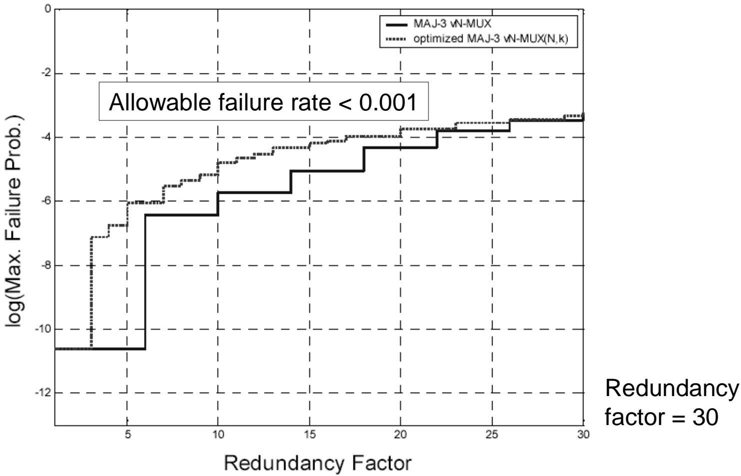

von Neumann Multiplexing with NAND2
I1
I2
Randomizer
Randomizer
Execution
Restoration # 1
Restoration # 2
Are classical fault-tolerance techniques practical for very high failure rates ?
Swiss Federal Institute of Technology
EPFL
Microelectronic Systems Laboratory
LSM

von Neumann Multiplexing with MAJ-3



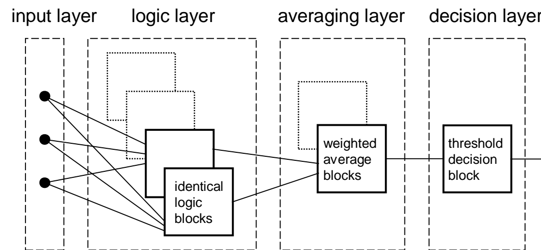
Alternative technique using majority multiplexing.

The maximum allowable device failure rate remains low…



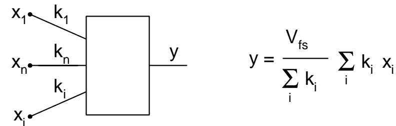
Redundancy factor = 30

Robust Design of Boolean Operators: Weighted Averaging



Fault tolerant architecture based on multiple layers

- Schmid and Leblebici, IJCNN 2003
- Schmid and Leblebici, ISCAS 2004



$$y = \frac{V_{fs}}{\sum_i k_i} \sum_i k_i \, x_i$$

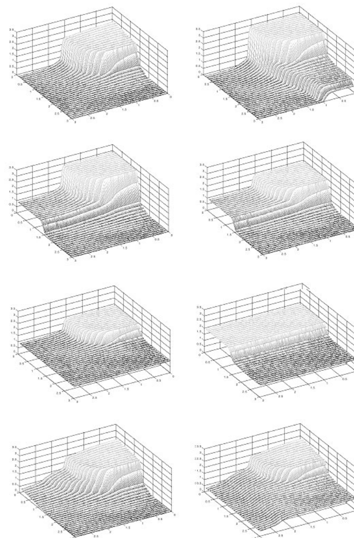
General weighted averaging and re-scaling function used in the third layer

Robust design of Boolean operators

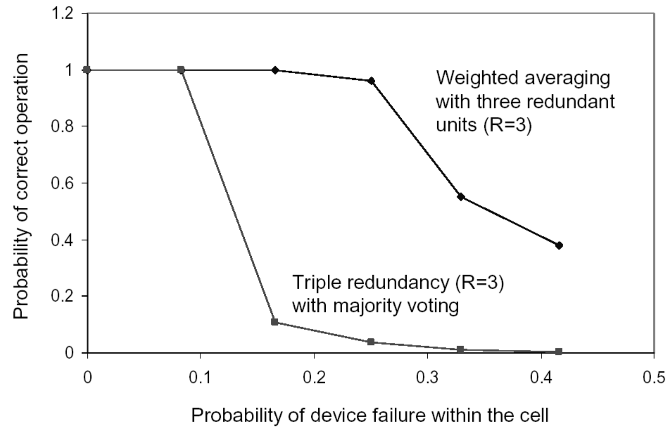
Output transfer function of the two-input NOR circuit, with three redundant units:

- **(a)** **one device failure in the 2nd layer**
- **(b)** **one failure in the 2nd layer**
- **(c)** **two failures in the 2nd layer**
- **(d)** **four failures in the 2nd layer**
- **(e)** **two failures in 3rd layer**
- **(f)** **four failures in the 2nd layer and one failure in the 3rd layer**
- **(g)** **two failures in the 2nd layer**
- **(h)** **four failures in the 2nd layer**

In most cases, the correct output function can still be obtained by applying the proper threshold decision in the fourth layer.

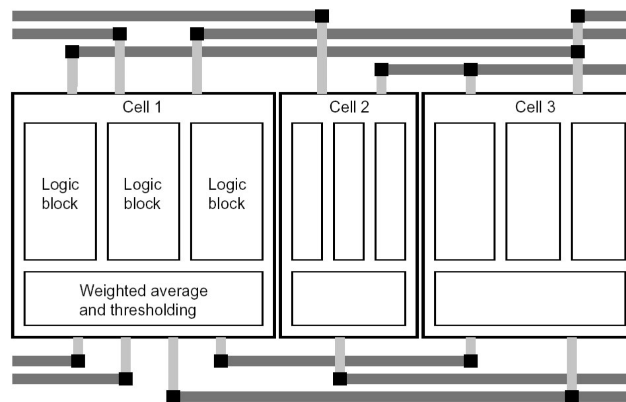


NOR2 Example: Three Redundant Units

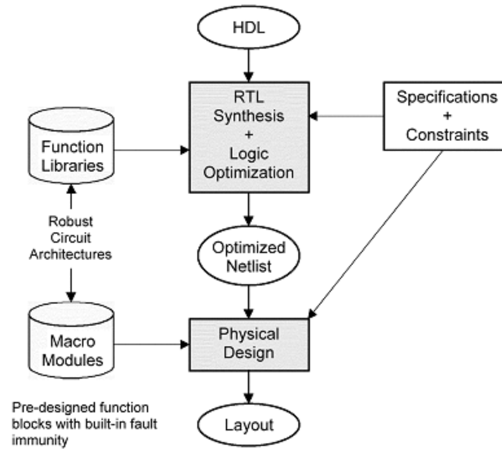


Probability of correct operation as a function of device failure rate

Standard-Cells with Built-in Fault Tolerance ?

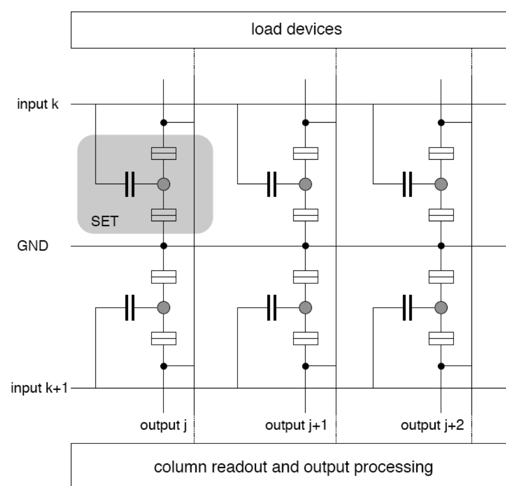


Simplified Design Flow

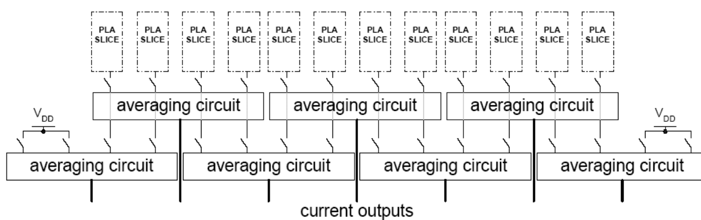


Simplified design flow incorporating pre-designed robust macro libraries

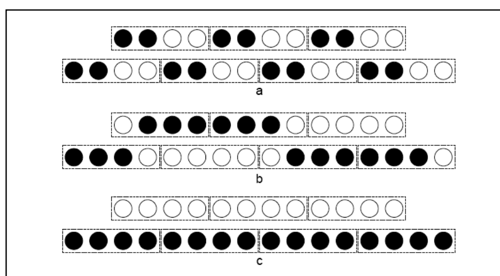
Programmable Logic Arrays with Fault Tolerance ?



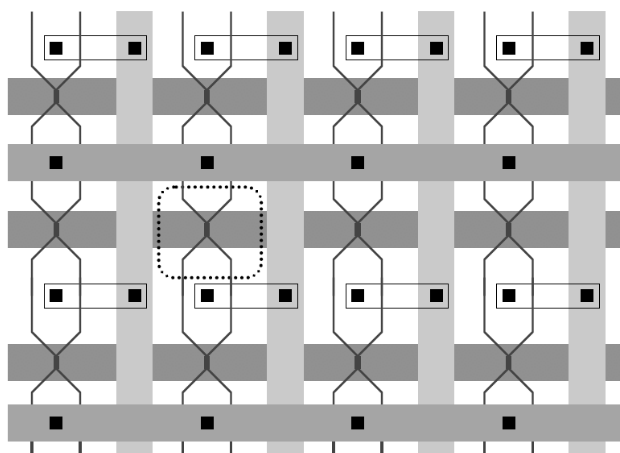
Programmable Logic Arrays with Fault Tolerance ?



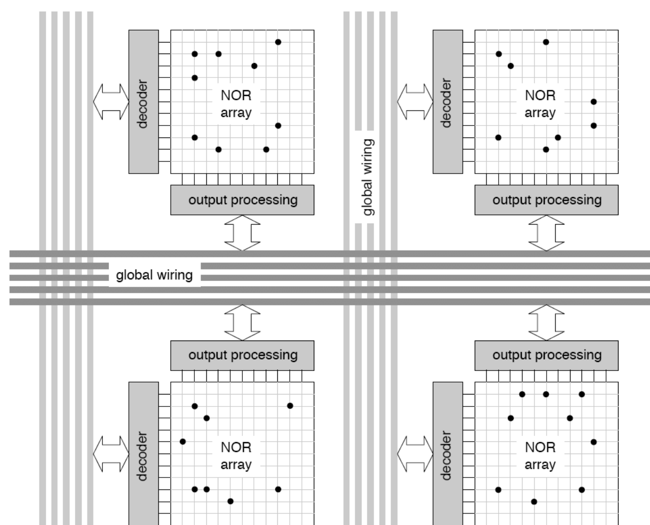
Configuration patterns for different levels of redundancy.



Close-up View of SET-based PLA



System Architecture



The Emerging Picture: Some Observations

- Comprehensive measures needed to ensure system robustness both for nanometer CMOS and for “novel” device technologies.
- Co-existence or combination of CMOS and “novel” technologies likely, to exploit complementary advantages.
- Design paradigm must conform to existing standards (design flow) in order to gain widespread acceptance.
- Array-based system architectures may have some advantages in terms of structural regularity, reconfigurability, and fault tolerance.
- No “silver bullet” solution: Design approaches are likely to rely on a combination of measures implemented at different levels of system hierarchy.