NC STATE UNIVERSITY

Devices, Integration Technologies and Circuits for Molecular Electronics

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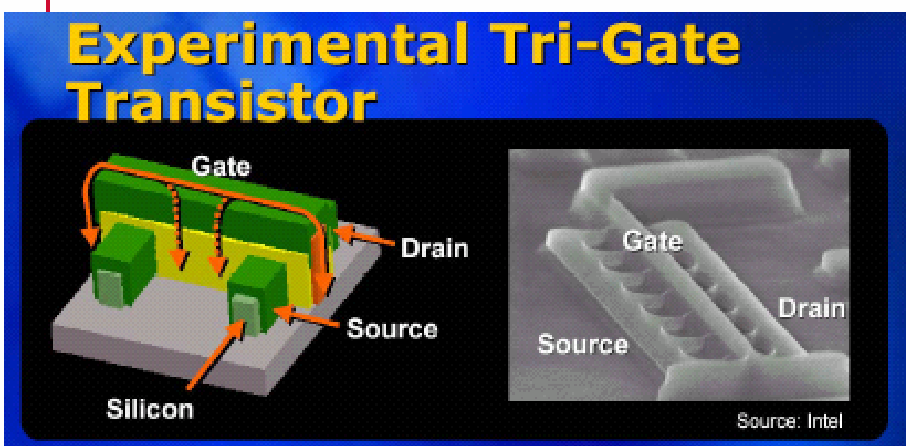
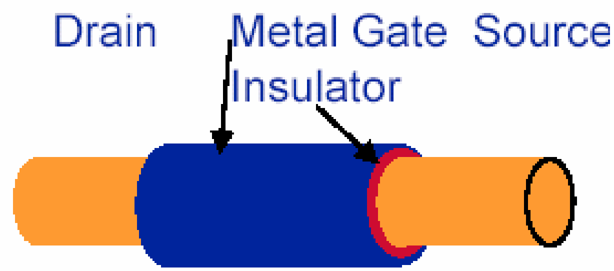
The End is Nigh!

- Last generation of CMOS
  - End of exponential growth
  - International Roadmap for Semiconductors
  - Predicted deployment by 2016
    - 22 nm "node"
    - 8 nm gate length



OR?



high electron mobility
(low effective mass)

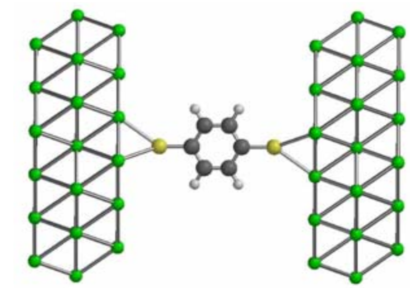
Outline

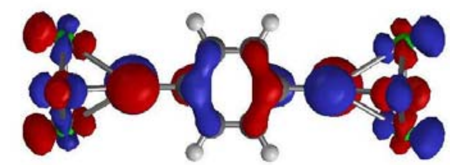
- **Devices**
  - Review and Status
- **Integration Technologies**
  - Crossbar
  - Nanocell
- **Circuit Issues**
  - Scalability of 1R and 1R1D RAMS
  - Logic Circuits

Molecular Memory Device Status & Mechanisms

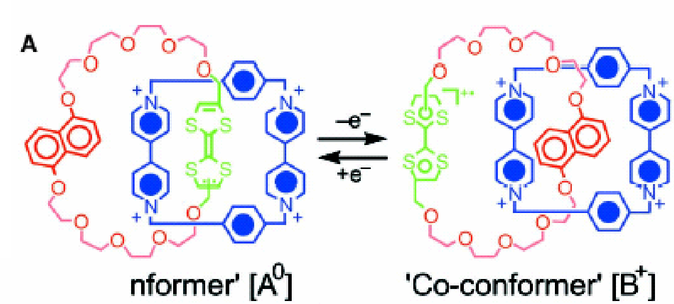
- Modulated tunnel diode
- Filament formation and opening
- Coulomb barrier formation and removal
- Electrochemistry-assisted capacitor

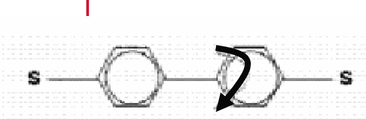
Tunnel Diode

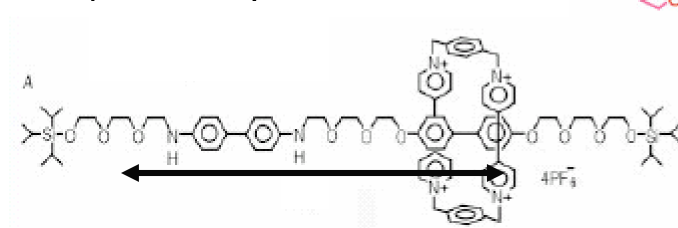




- **Metal-molecule-metal forms a tunnel diode**
- **Tunnel barriers modified via:**
  - Van-der-Waal's (electrostatic) interactions with neighbors
    - Interpreted from probe data
  - Covalent bond change (e.g. Redox)
    - Theoretical & Indirect evidence (Heath, others)
  - Mechanical change
    - Theoretical & indirect evidence (Stoddard, others)



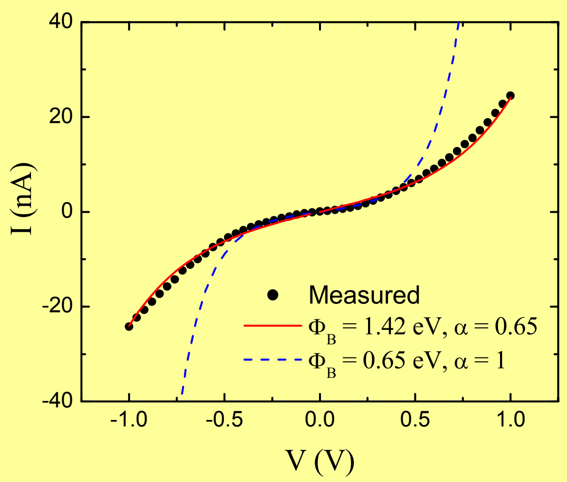


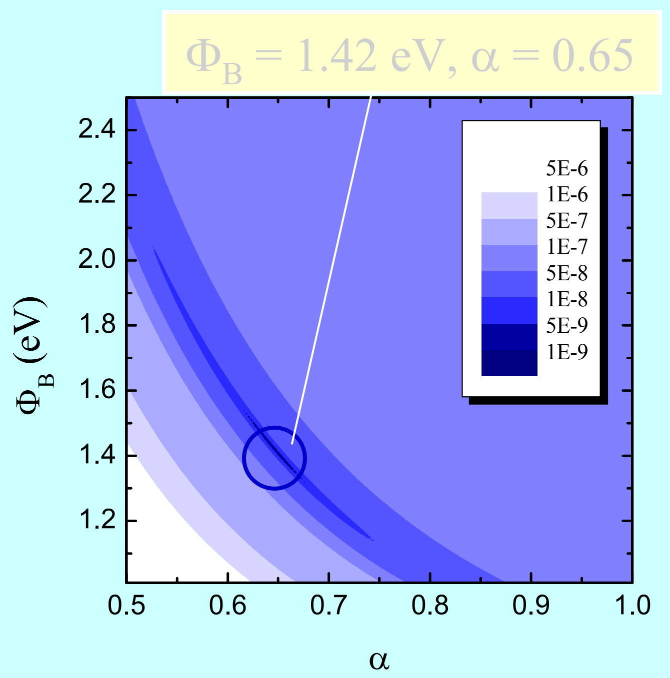


Tunnel Diode Verification (Reed)

$$J=\left(\frac{e}{4\pi^2\hbar d^2}\right)\left\{\left(\Phi_B-\frac{eV}{2}\right)\exp\left[-\frac{2(2m)^{1/2}}{\hbar}\alpha\left(\Phi_B-\frac{eV}{2}\right)^{1/2}d\right]-\left(\Phi_B+\frac{eV}{2}\right)\exp\left[-\frac{2(2m)^{1/2}}{\hbar}\alpha\left(\Phi_B+\frac{eV}{2}\right)^{1/2}d\right]\right\}$$

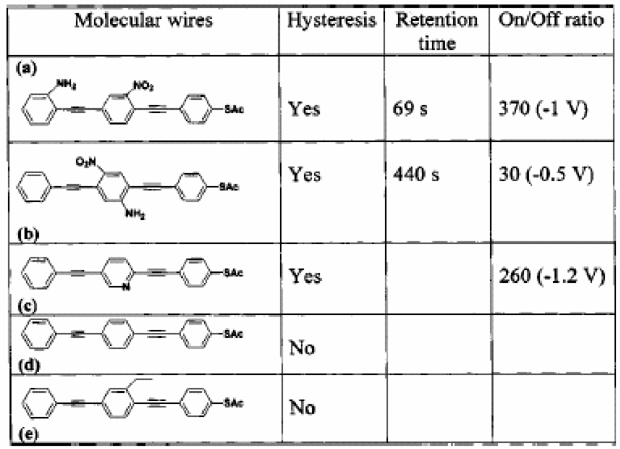
Minimized fits (nonlinear LSQ) to I(V) gives $\{\Phi,\alpha,\Delta)$





Multi-State Tunnel Diode?

- ▷ **With REDOX centers:**



Molecular wires	Hysteresis	Retention time	On/Off ratio
(a)	Yes	69 s	370 (-1 V)
(b)	Yes	440 s	30 (-0.5 V)
(c)	Yes		260 (-1.2 V)
(d)	No		
(e)	No		

FIG. 2. Molecular wires used. Molecules **a**, **b**, and **c** contain redox centers while molecules **d** and **e** do not contain such centers.

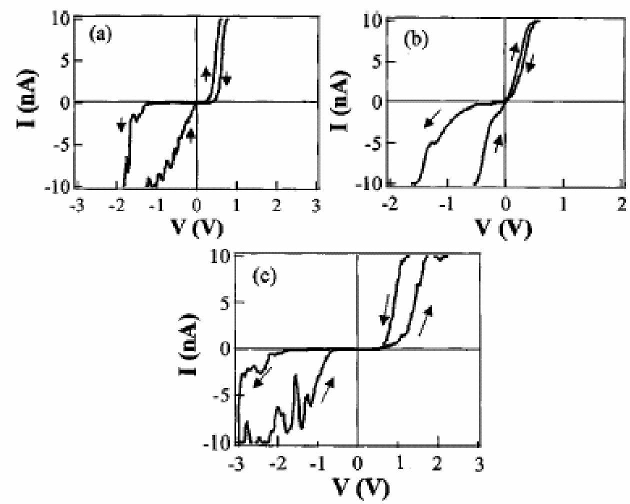
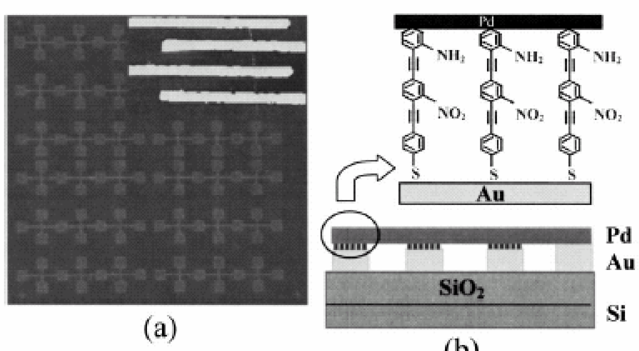


FIG. 3. Typical $I-V$ curves of molecular devices. (a), (b), and (c) correspond to molecules **a**, **b**, and **c** shown in Fig. 2, respectively.



Li. et.al, APL 82(4), 2003
(NASA, UCLA, Rice)
(used in ITRS 03)

NanoFilaments

- ▷ **Williams, Stoddart: Nano Letters, 4(1), 2004:**

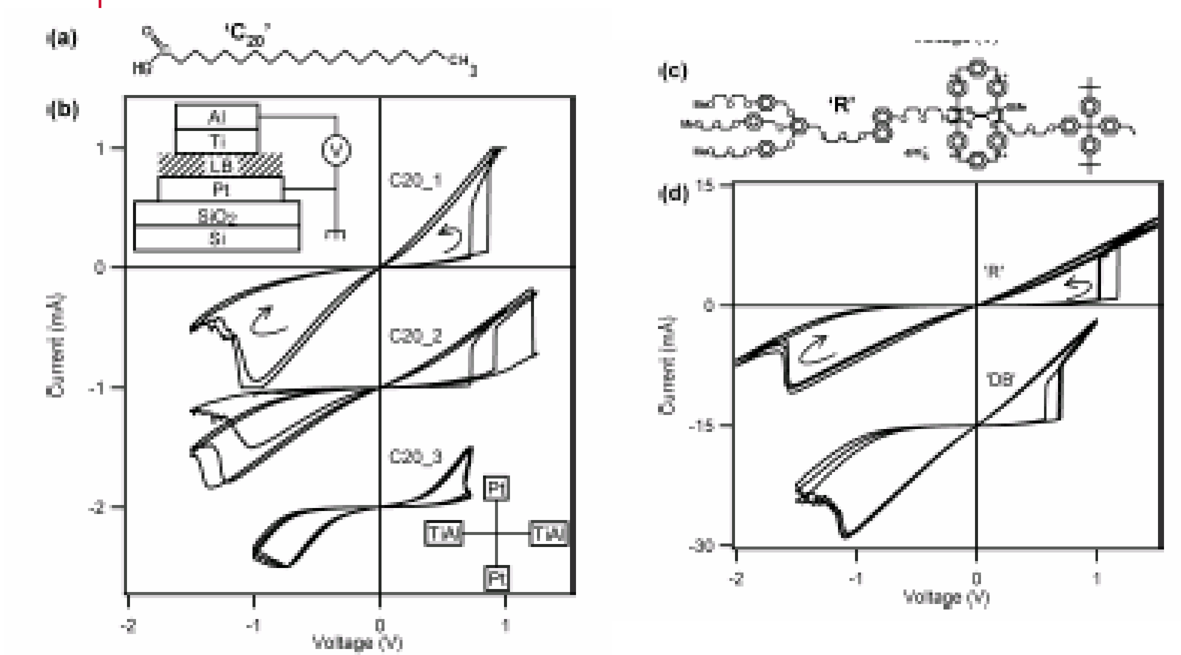


Figure 1. (a) Eicosanoic acid (C_{20}), (b) dc I–V measurements showing the "figure-8" hysteresis loops of three different C_{20} molecular monolayer devices. All sweeps follow the direction of the arrows. Successive curves are offset −1 mA. All devices are a sandwich structure of 100 nm-Pt/LB monolayer/5 nm-Ti, 200 nm-Al (inset, top). All voltages are applied w.r.t. the grounded Pt electrode. These measurements are from 1 × 1 junctions with planar areas of 10, 10, and 7.5 μm^2 (inset, bottom). (c) [2]rotaxane **R**. The dumbbell-only molecule **DB** is identical to **R** minus the captive cyclophane ring. (d) dc voltage-bias measurements of one [2]-rotaxane "R" device and one dumbbell "DB" device, of areas 25 and 50 μm^2. Curves DB are offset −15 mA. All data at 300 K.

•>125 day retention
•>1 V variation
•Ron:Roff ~ 100 - 200

- ▷ **Proposed mechanisms:**
  - ◆ Molecule/metal interaction; Nanofilament; "incomplete electrochemical reaction at electrode"

Nanofilaments

- Tour, Franzon, et.al. JACS 2003

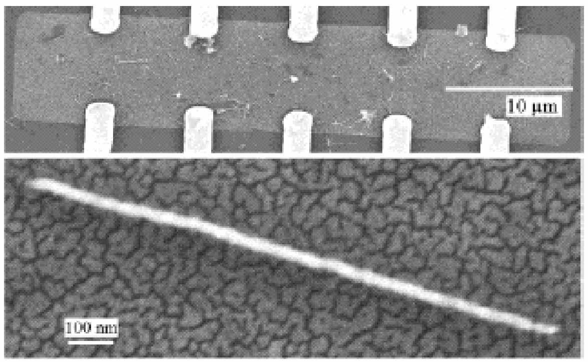
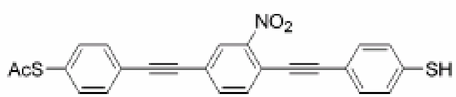


Figure 1. SEM image of the NanoCell after assembly of the Au nanowires and **1**. The top image shows the five juxtaposed pairs of fabricated leads across the NanoCell, and some Au nanowires are barely visible on the internal rectangle of the discontinuous Au film. The lower image is a higher magnification of the NanoCell's central portion showing the disordered discontinuous Au film with an attached Au nanowire, which is affixed via the OPE-dithiol (not observable) derived from **1**.

electrodes (≤1 picoamp up to 30 V). In this study, each juxtaposed pair serves as an independent memory bit address system.



1

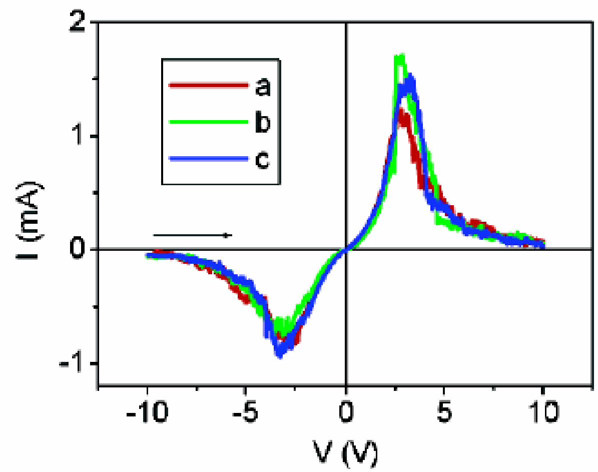


Figure 2. $I(V)$ characteristics of the NanoCell at 297 K. Curves a, b, and c are the first, second, and third sweeps, respectively (~40 s/scan). The PVRs in curve c are 23:1 and 32:1 for the negative and positive switching peaks, respectively. The black arrow indicates the sweep direction of negative to positive.

remove the acetyl group.[17] A chip containing 10 NanoCell structures was placed in the vial (active side up), and the vial was further agitated for 27 h to permit the nanowires to interlink the discontinuous Au film via the OPEs (Figure 1). The chip was removed, rinsed with acetone, and gently blown dry with N_2.

Sakamoto, et.al., APL 82(18) 2003
(NEC & NIMS)

NanoFilament

- **In solid electrolyte**
  - Mechanism: Precipited Cu atoms forming conducting paths
  - 100 μS write times; Ron:Roff 10^6
  - Retention > several months
  - Demonstrated several months retention time, consistent results across array, 10^3 - 10^5 cycles, decreasing with smaller size

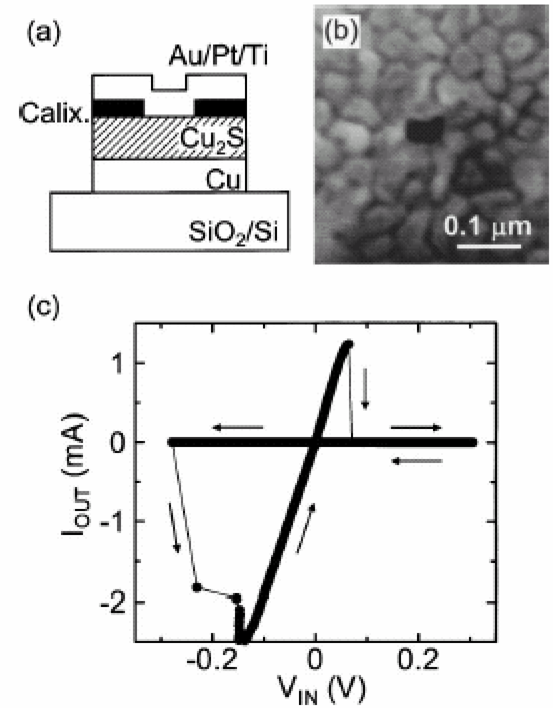
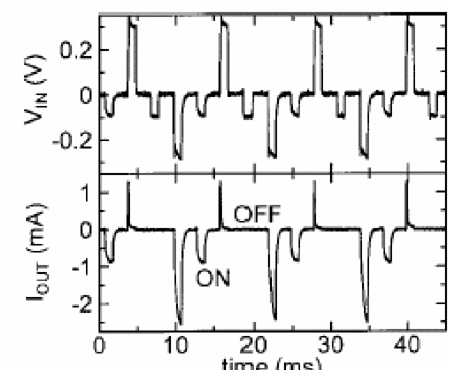


FIG. 1. (a) Schematic view of nanometer-scale switch using a Cu_2S film sandwiched between Cu film and a top electrode (Au/Pt/Ti). (b) Plane view of top electrode with a hole in the center. (c) Current–voltage characteristics of the device with a 0.03 μm hole.



Coulomb Barrier

- Bozano, et.al., APL 84(4), 2004. (IBM)
  - "… due to charge storage, where resultant space-charge field inhibits injection." (on Al grains)
  - Don't claim a device (yet)

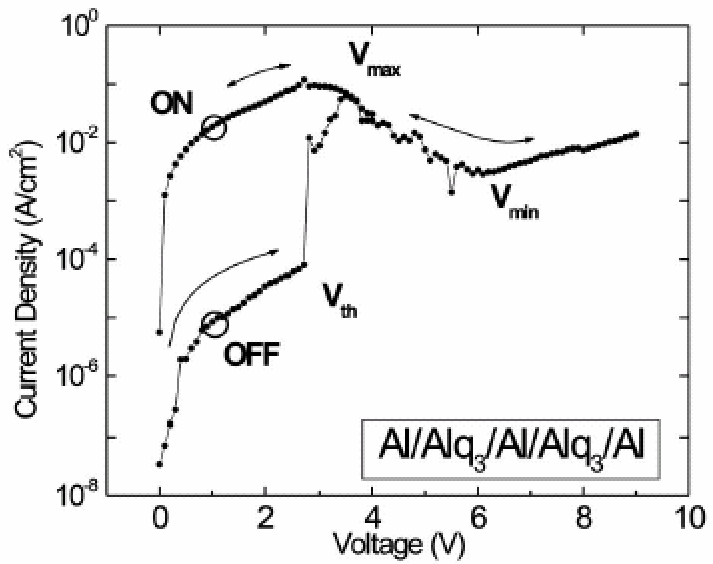


FIG. 3. Current–voltage characteristic of an Al (50 nm)/Alq_3 (50 nm)/Al (5 nm)/Alq_3 (50 nm)/Al (50 nm) device. The fundamental parameters of the bistable behavior are indicated. The ON and OFF states are set at voltages close to V_{max} and V_{min}, respectively, and read at 1 V. The transition from the OFF to the ON state occurs at the threshold voltage (V_{th}).

Electrochemical Capacitor

- ▷ **Lindsay et.al, (NCSU / ZettaCore)**
  - ◆ Multi-state “capacitor” based on electrochemistry
  - ◆ 200s retention time
  - ◆ IV results modeled from CV measurements

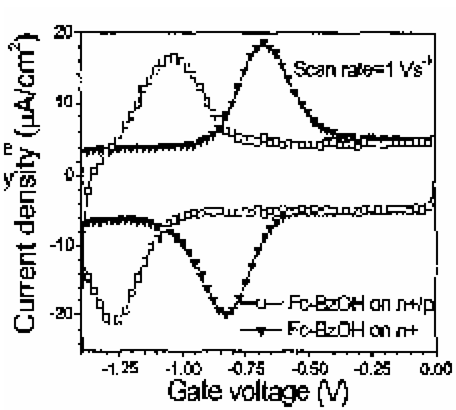


Figure 7a CyV of Fc-BzOH on n+ and n+/p diode: effect of forward-biased diode characteristics on redox peak potentials. Doping density of the n+ region is in the order of 1×10^{21} cm^{-3}.

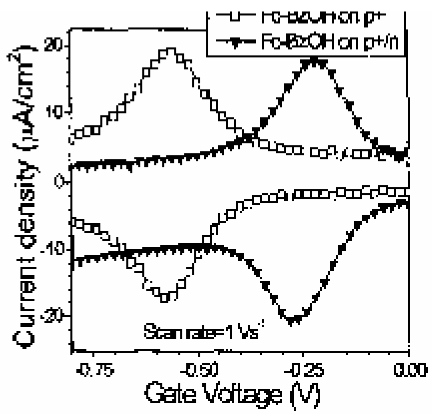
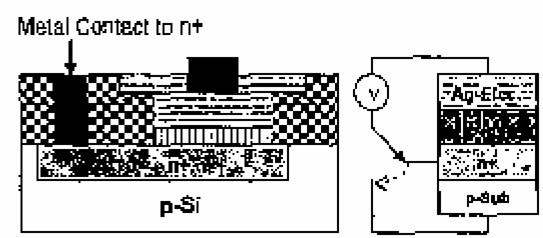


Figure 7b CyV of Fc-BzOH on p+ and p+/n diode: effect of reverse-biased diode characteristics on redox peak potentials. Doping density of the p+ region is in the order of 1×10^{21} cm^{-3}.



Misra et.al., IEDM 2003

Outline

- **Devices**
  - Review and Status
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  - Crossbar
  - Nanocell
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  - Scalability of 1R and 1R1D RAMS
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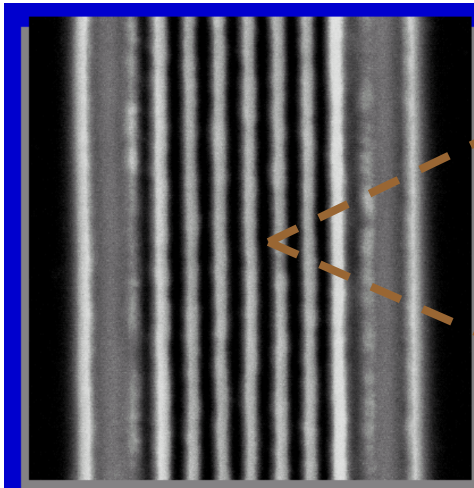
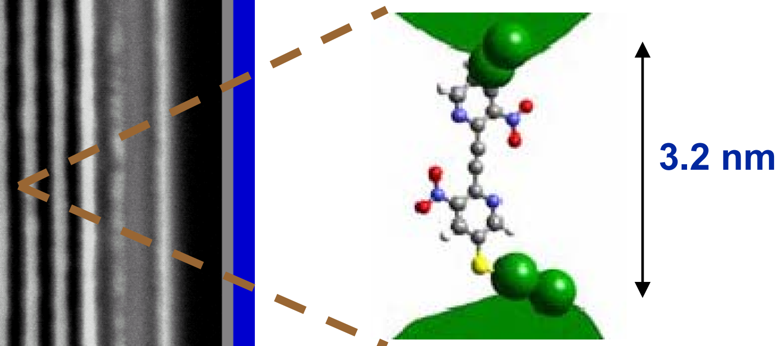
Integration Problem Statement

- **Scale mismatch:**

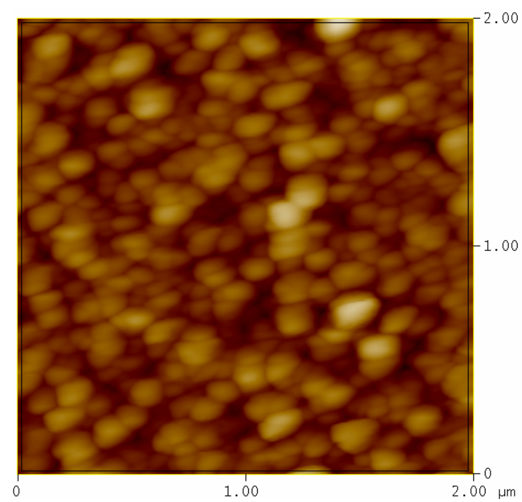
c/- Intel



50nm Lines Printed with EUV Lithography



- **Solution Paths**
  - Directed Nano-imprinting
  - Random interconnect



Limited Metal Smoothness

Directed NanoImprint

- **Nano-imprinting**
  - E.g. Heath:

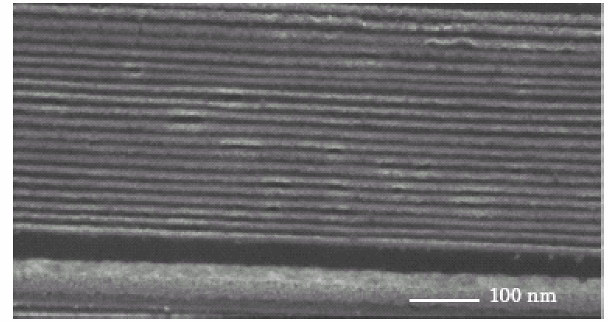
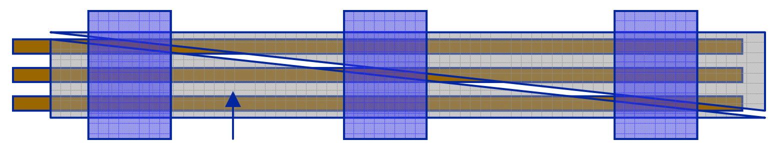
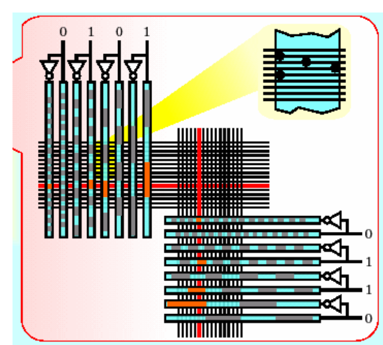


Figure 2. Array of nanowires, each approximately 5 nm in diameter. The lattice constant is 15 nm. Certain materials parameters important to solid-state devices, such as the average density of dopant atoms, no longer hold meaning at these nanoscale dimensions. At this size scale, however, chemical control over molecular properties is highly developed.

- **Fanout to Microscale**
  - Random angled alignment & Nano-imprinting
  - Franzon, DiSpigna:



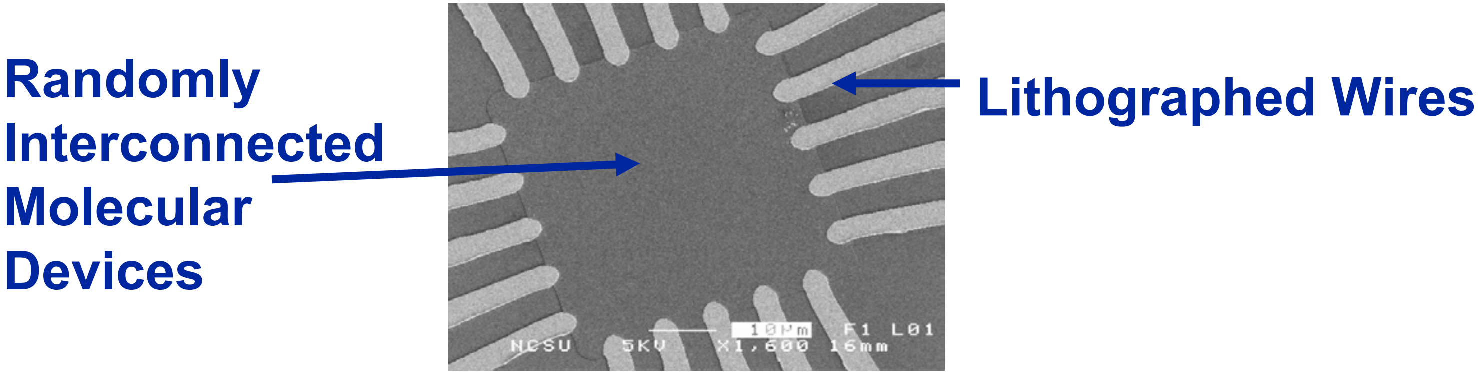
- **Integrated devices into wires**
  - DeHon:



Random Interconnect

NanoCell Concept

- (with Jim Tour's group @ Rice University)
- Physical Architecture:



- Build logical architecture by programming device externally, as a complete unit

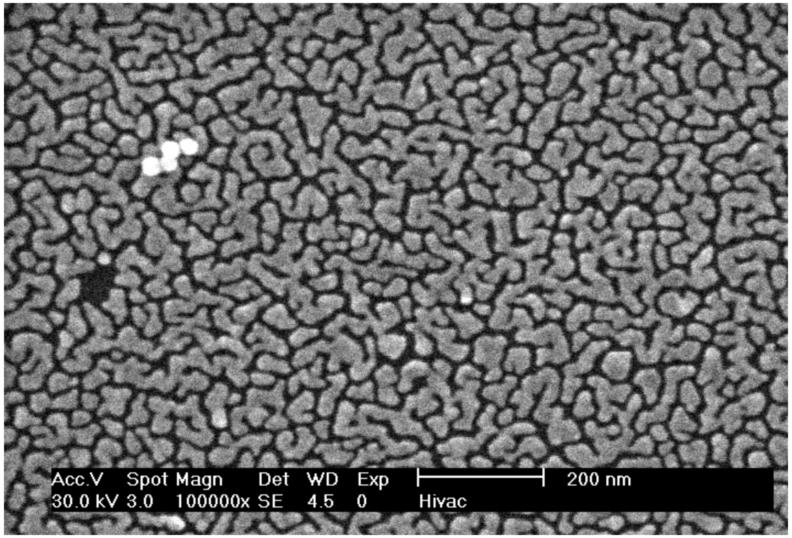
Tour, J.M., Cheng, L., Nackashi, D.P., Yao, Y., Flatt, A.K., St. Angelo, S.K.; Mallouk, T.E.; Franzon, P.D.; "Nanocell Electronic Memories," J. Am. Chem. Soc., **125, 13279-13283, 2003.**

J.M Tour, W.L. Van Zandt, C.P. Husband, S.M. Husband, L.S. Wilson, D.P. Nackashi, P.D. Franzon, "Nanocell Logic Gates for Molecular Computing," IEEE Trans. Nano**., vol 1, June 2002, pp. 100-109.**

NanoCell Construction

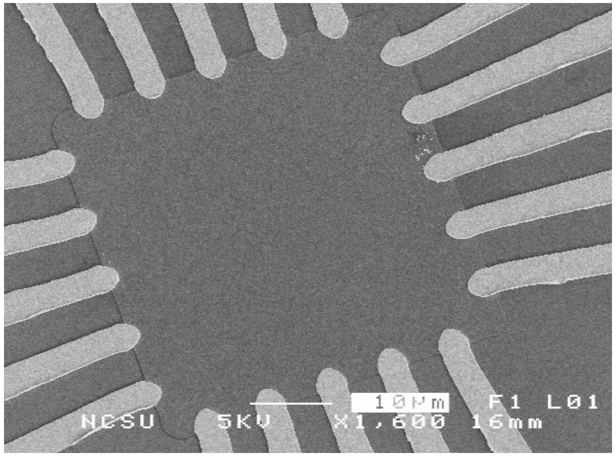
Discontinuous Gold Film deposition and patterning

- Thin gold evaporation

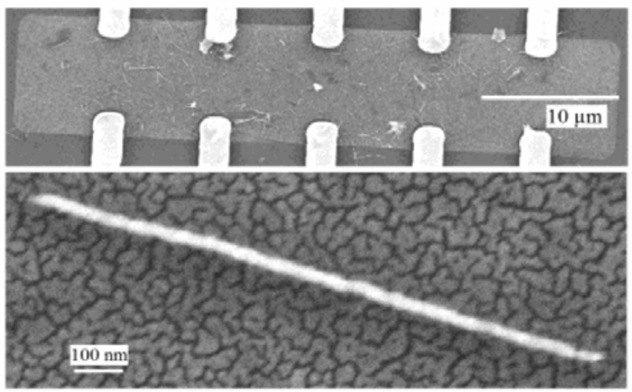


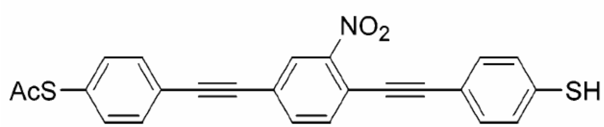
Pattern electrodes:

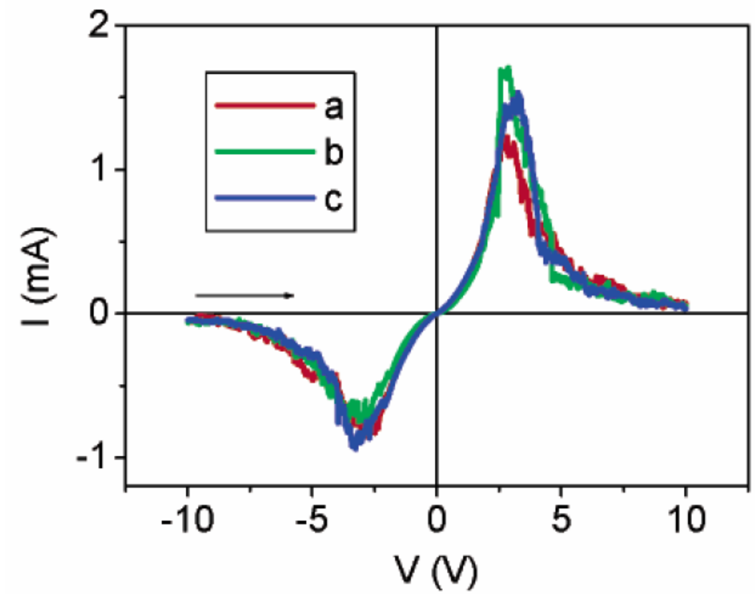
- 2-step liftoff to prevent edge shorting



Assembly and Characterization

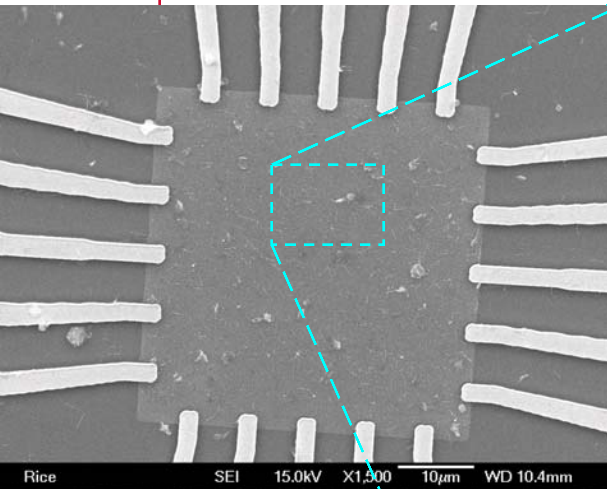


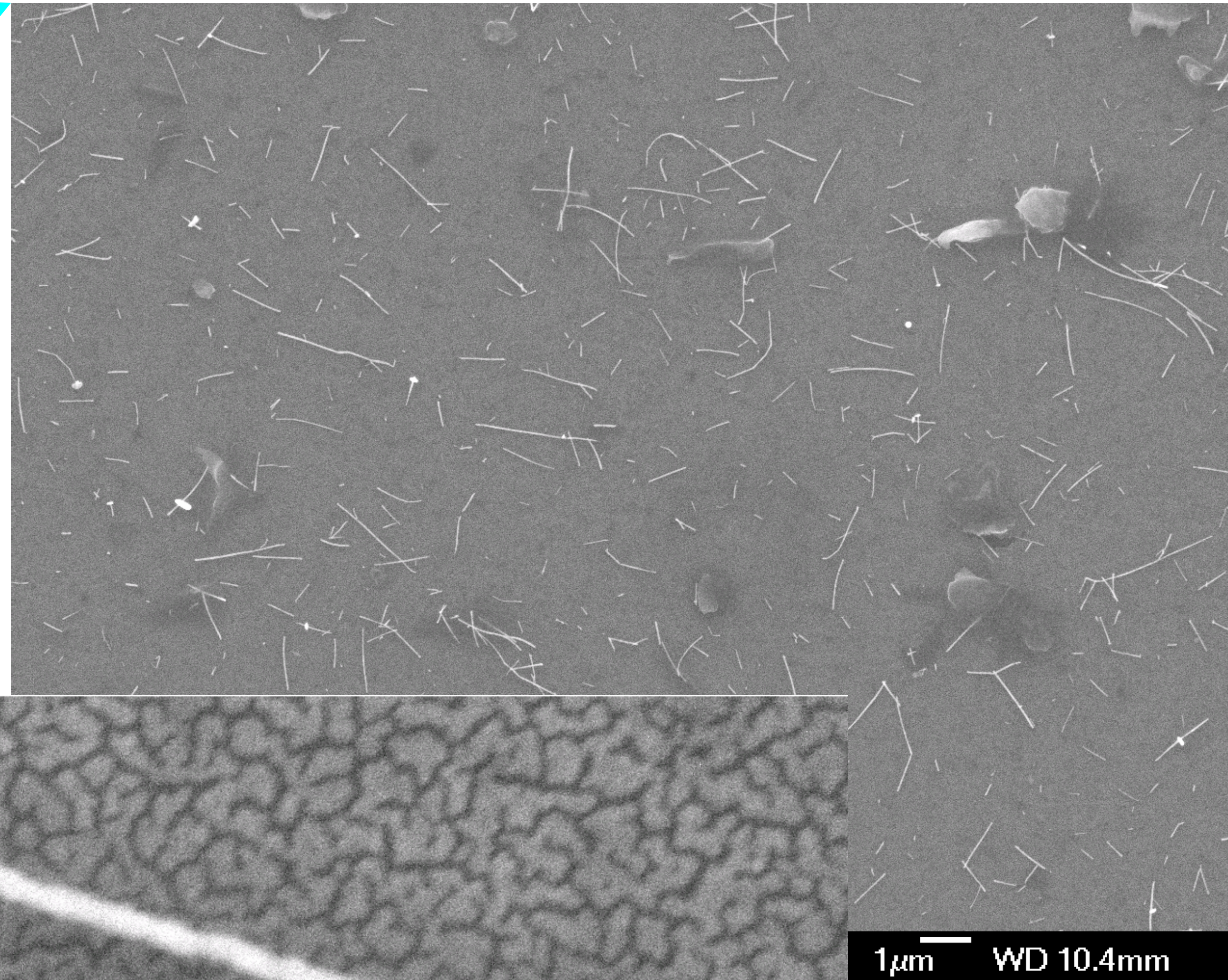


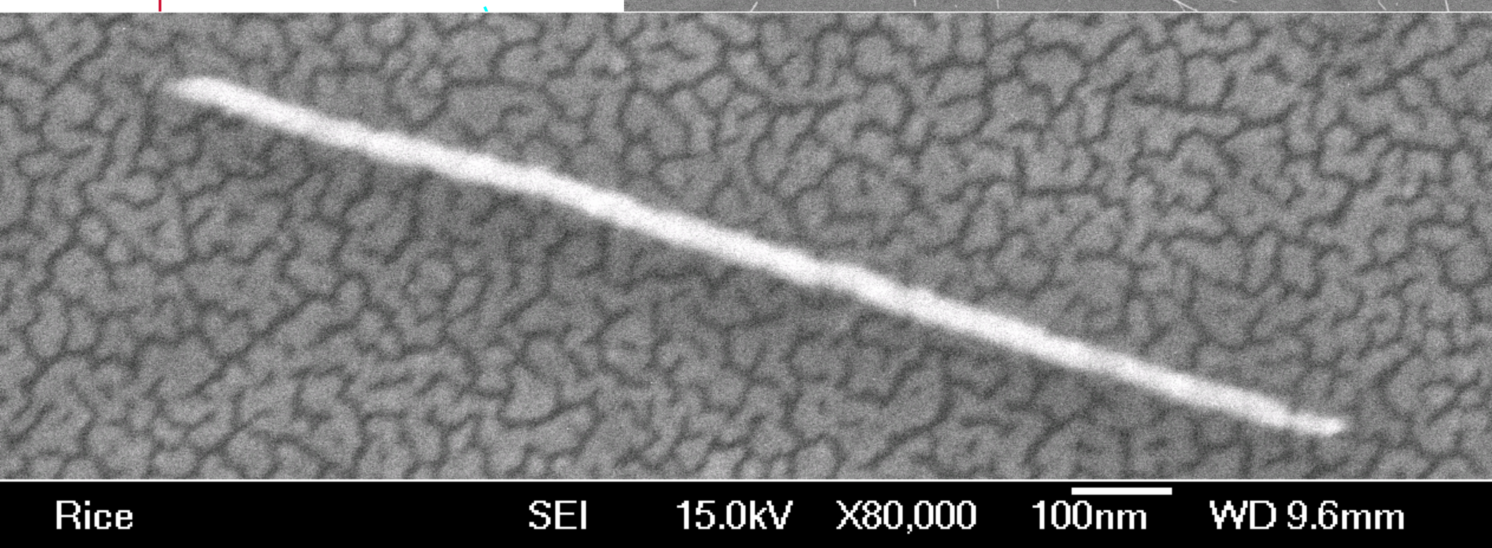


- **UV-ozone and EtOH wash**
- **Gold nanorod passivation and assembly**
  - 200-2000nm rods, mononitro oligo(phenylene ethynlene) + DCM
  - Thioacetyl cleaved in NH_4OH + EtOH
- **Nanocell chip added for assembly**

Assembled NanoCells



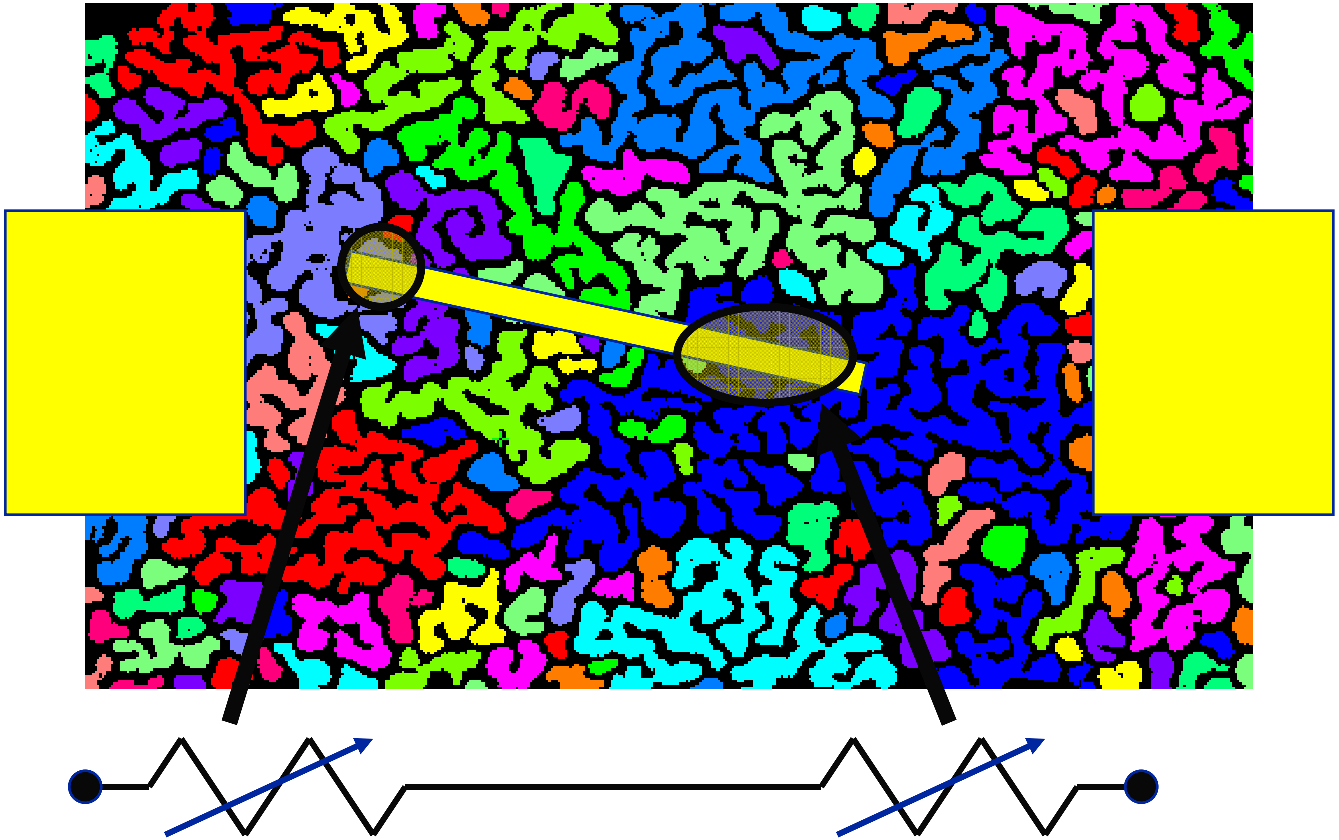




with:
L. Cheng, J. Tour

After Assembly

- Randomly connected circuit built!



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  - Crossbar
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- Circuit Issues
  - Scalability of 1R and 1R1D RAMS
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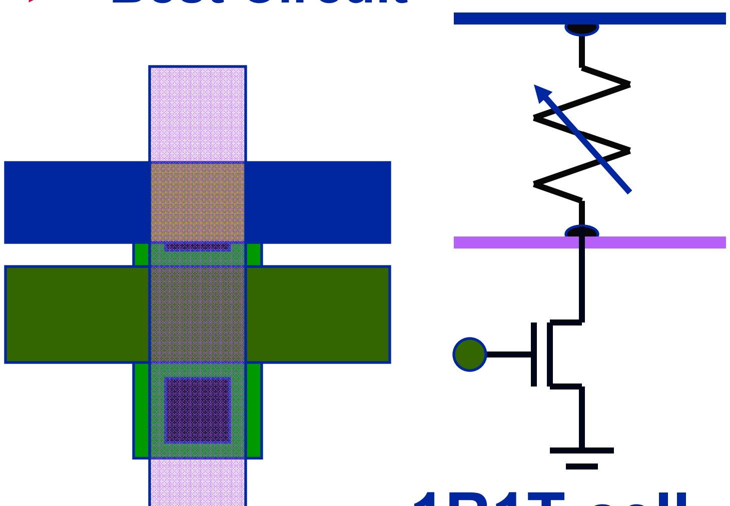
Memory and Crossbar Architectures

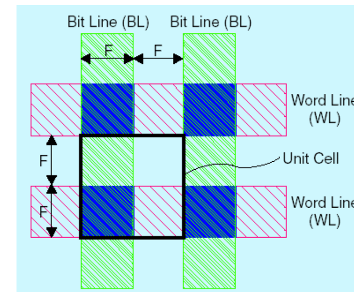
1R1T Cell:

- Conventional (MRAM-style) architecture
- Large Cells
- Best Circuit

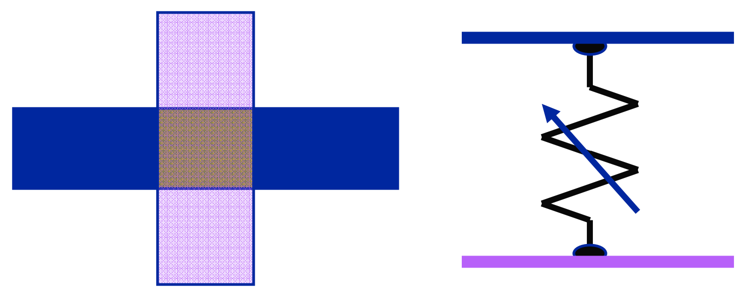


1R1T cell

1R Cell:



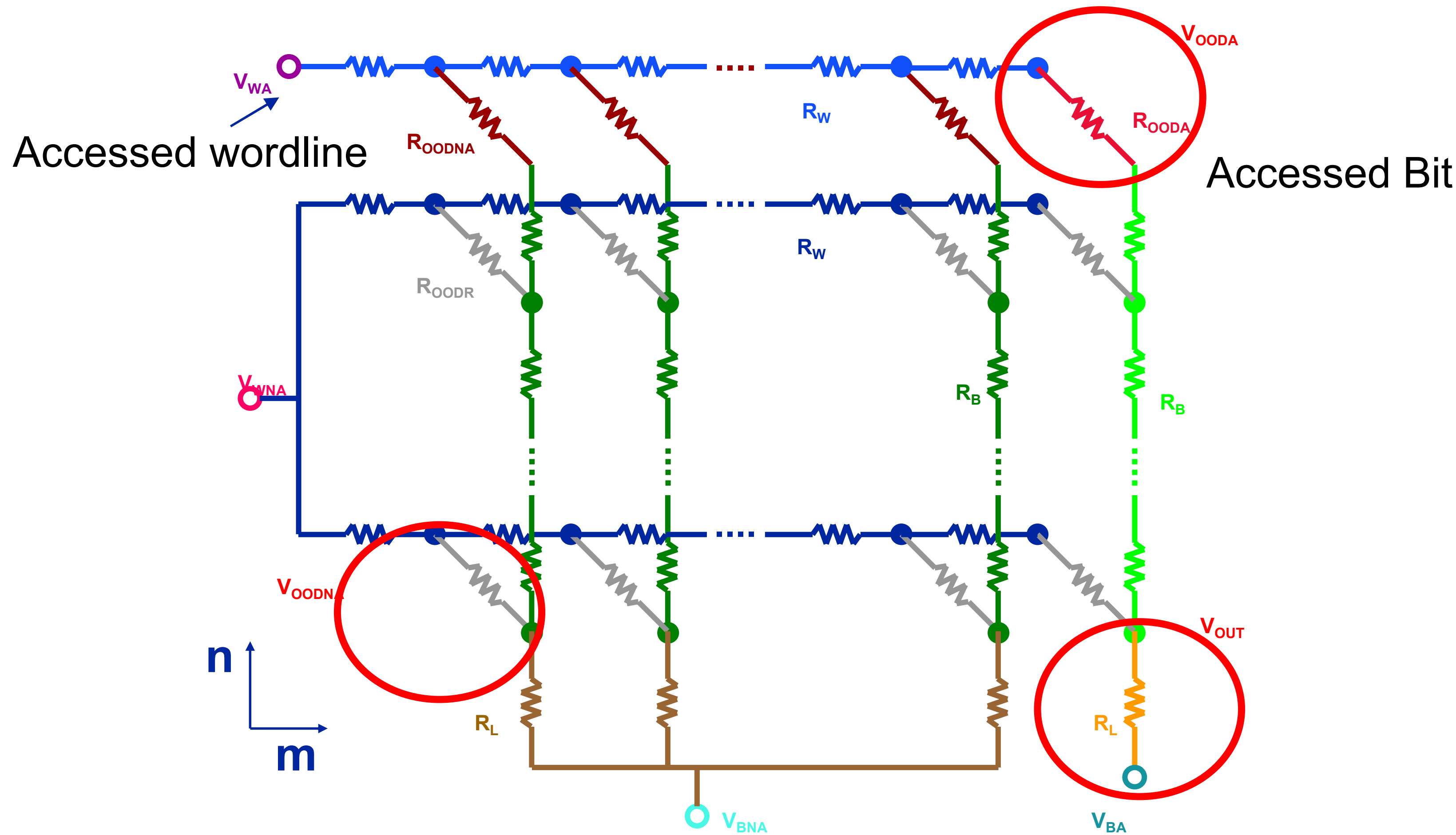
- All demonstrated Molecular RAMs
- Smaller Cells
- More difficult circuit
  - Reduced Isolation
  - Slower performance



1R cell

Molecular-scale Transistor Difficult

Scalability issues in 1R RAMs

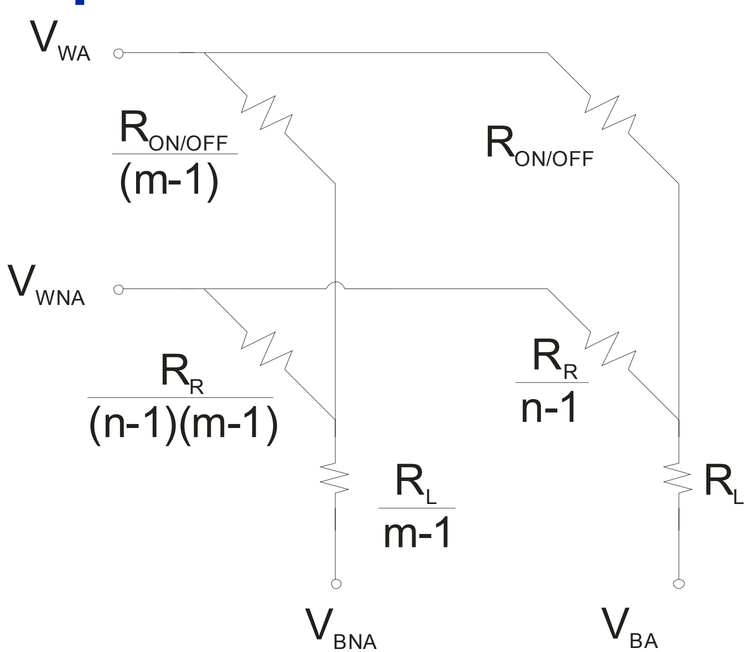


Should be "quiet"

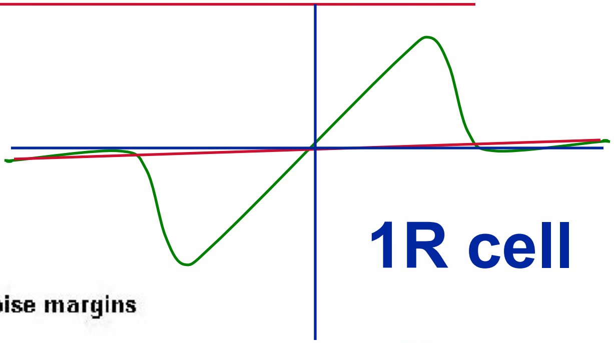
Bit Read/Write

Typical Parameters

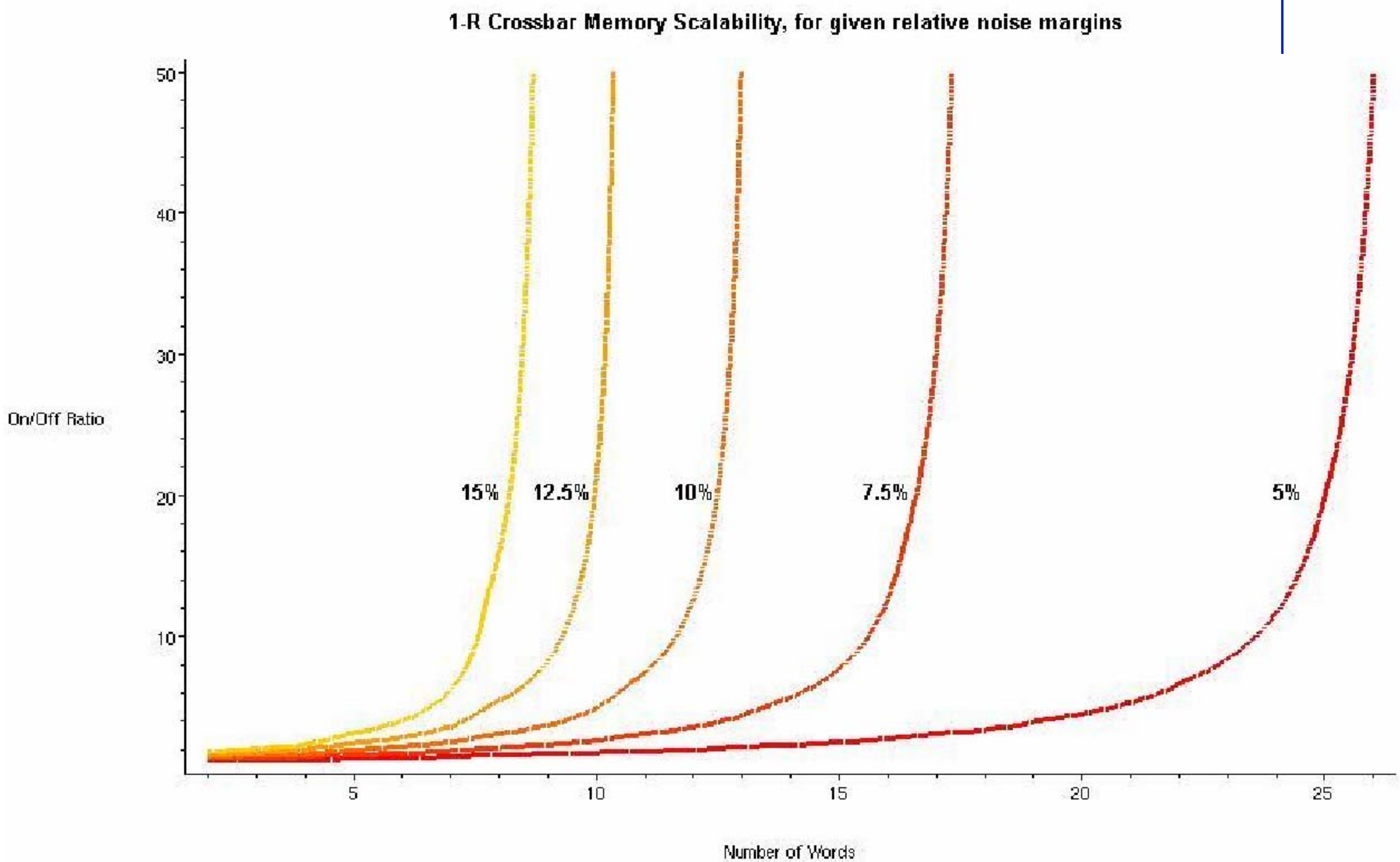
- **Rwire << Rdevice**
  - E.g. 40 nm x 8 nm x 1 μm wire : ~ 3 kΩ
  - 40 nm x 40 nm Molecular Device:
    - Ron ~ 10 MΩ; Roff ~ 1 GΩ
- **Permits simplification of resistance model**



Noise Margin Scaling



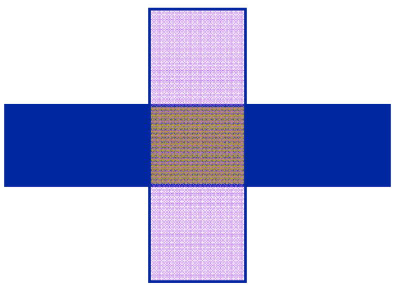
1R cell



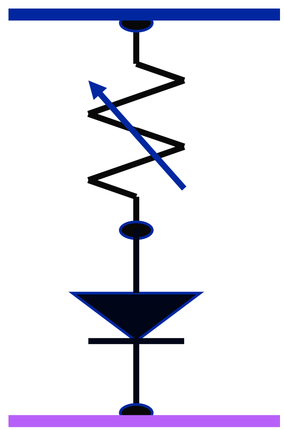
16x16 array (256 bits)

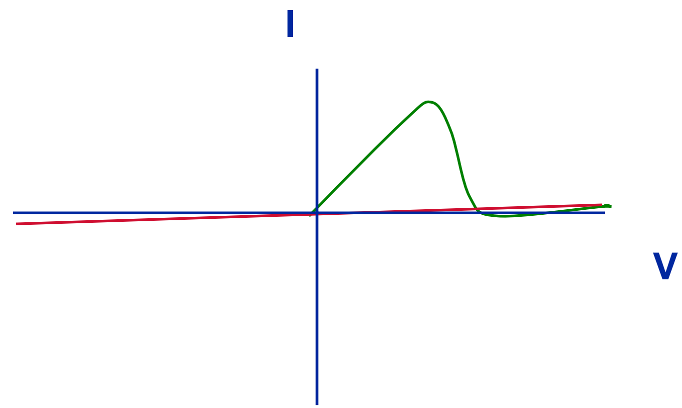
Better Approaches

- 1R1D Cell : Reverse bias isolation required to build a scalable array



1R1D cell





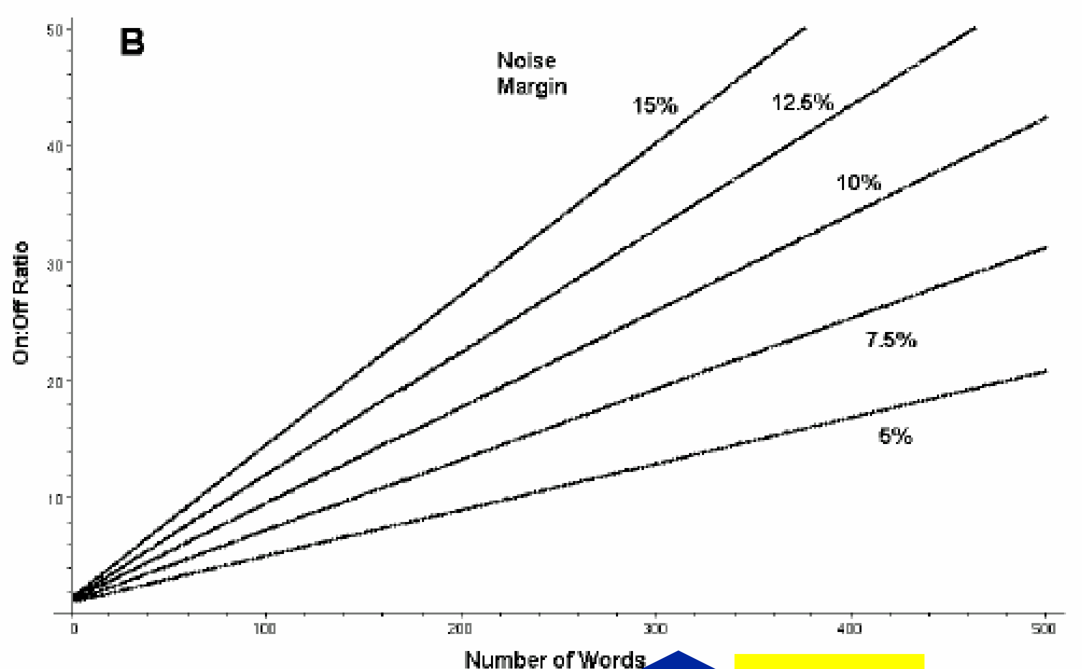
- High-Z sense Amps & other circuit approaches can help scalability

Noise Margin Scaling for 1R1D cell

- Noise margin:

$$NM = \frac{\sqrt{k}(k^{\frac{3}{2}}V_{WLA}n + k^2V_{WLA} + \sqrt{k}V_{WLNA}n - k^2V_{BLA} - \sqrt{k}V_{WLA}n - kV_{WLA} - k^{\frac{3}{2}}V_{WLNA}n + kV_{BLA}}{(k^{\frac{3}{2}} + \sqrt{k}n + k)(\sqrt{k} + \sqrt{k}n + k)}$$

On:off Ratio	Max. Array
7:1	64x64
13:1	128X128
100:1	1225X1225
1000:1	12kX12k
8000:1	1MX1M

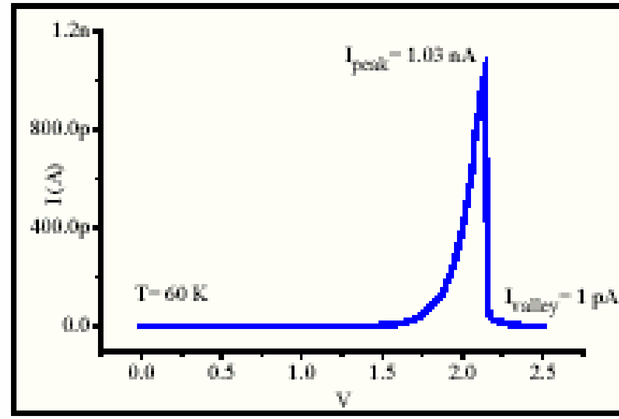


100kb

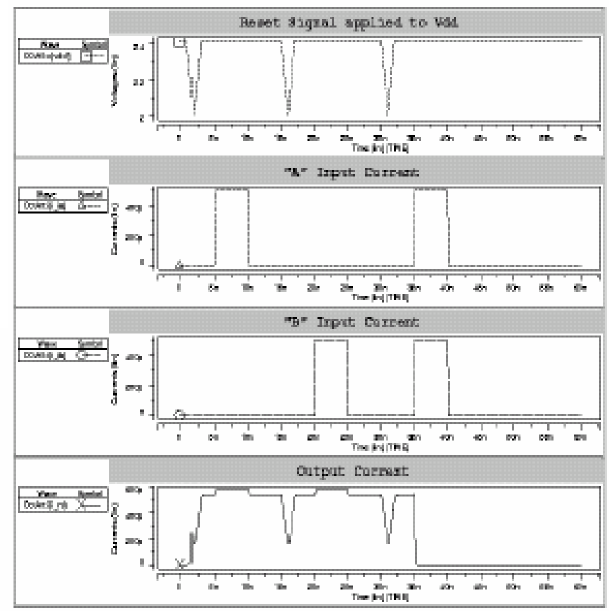
Impact of Scalability

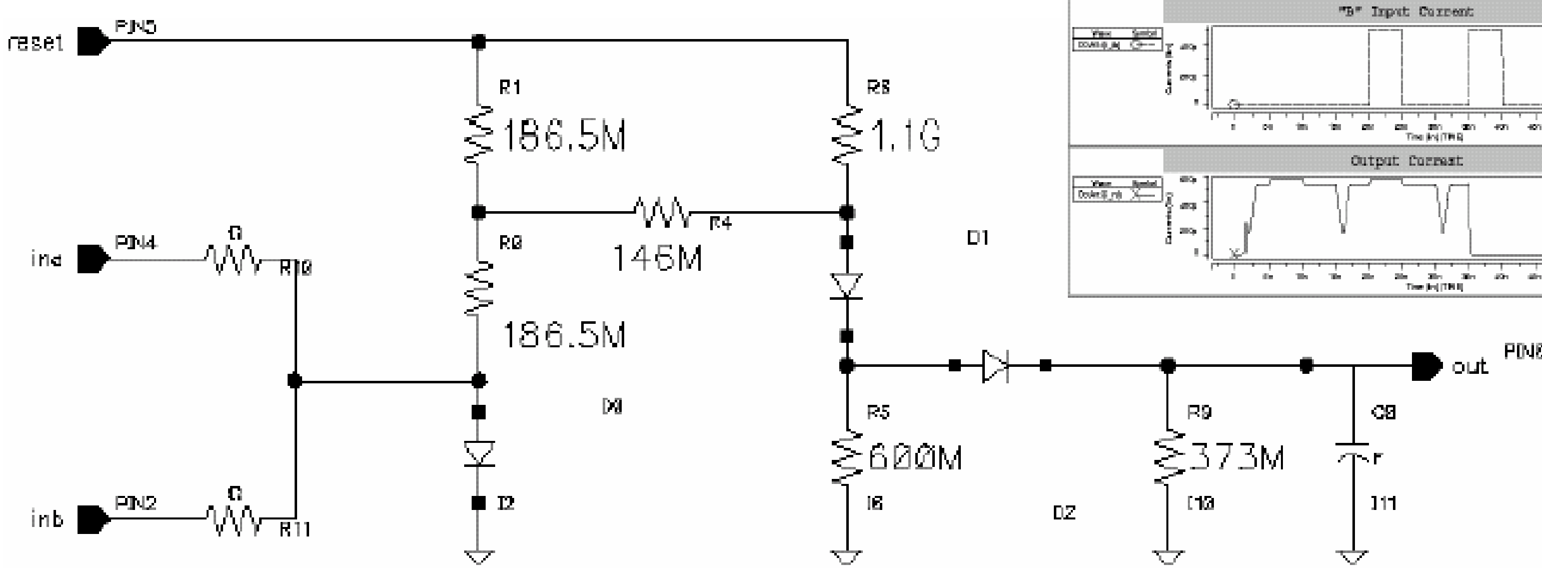
- **Raw Bit Density**
  - $4F^2$ cells; F = 5 nm ➔ 10^{12} bits / sq.cm = 100 DVDs/sq.cm.
- **Effective Bit Density**
  - Circuit overhead determined by size of Memory Subarray
  - Large subarray ➔ Less area overhead for fanout, row/column decoders and sense amps
  - Typical DRAMs organized as arrays of 128 Mbit (10,000 x 10,000) 1R1T cells
    - 6,400 bits / edge circuit
  - 1000:1 on:off ratio needed to match DRAM

Logic



- Scalable logic difficult with two terminal devices
- E.g. NAND gate based on NDR





Conclusions

- ▷ **Potential of Molecular Electronics**
  - Mainly Ultra-dense flash memories
  - 10^{12} bits/sq.cm. ➔ Video Library in flash card!
  - Potential exists BEYOND the end of ITRS (~2016+)
- ▷ **Devices**
  - True molecular basis demonstrated and understood
  - Performance still needs substantial improvement though
- ▷ **Integration & Interconnect**
  - Critical challenge!