National Science Foundation

Emerging Nanotechnologies for Computing

ISCAS
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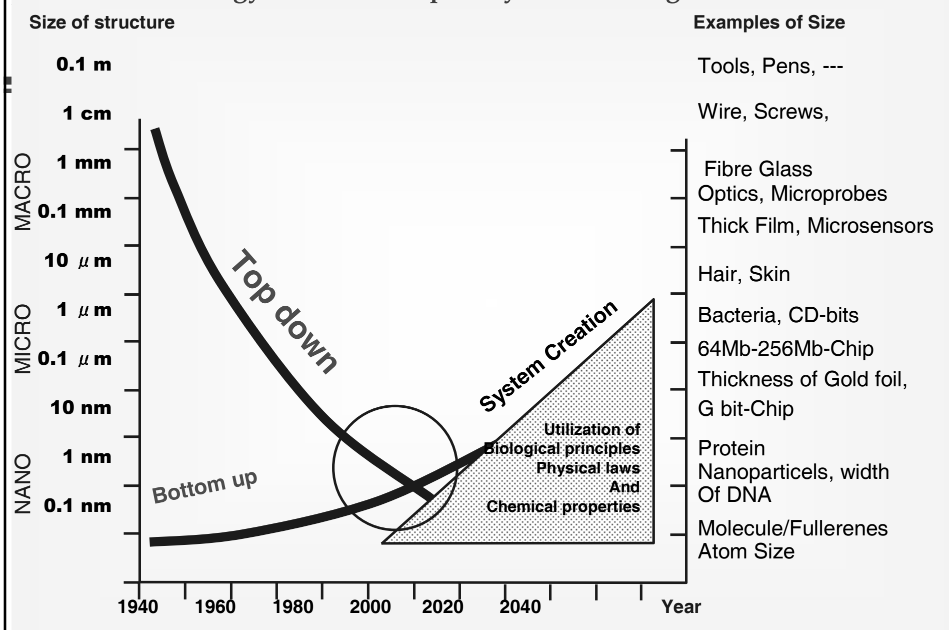
National Nanotechnology (NNI) Initiative

Create materials, devices and systems with fundamentally new properties (because of their small structure) at atomic, molecular levels in the length scale of approximately 1–100 nm range.

- **10 Year vision, 3 years into the program**
- **16 US federal agencies involved**
- **Significant impact on microelectronics expected in the long run**

Nanotechnology: an Interdisciplinary Undertaking



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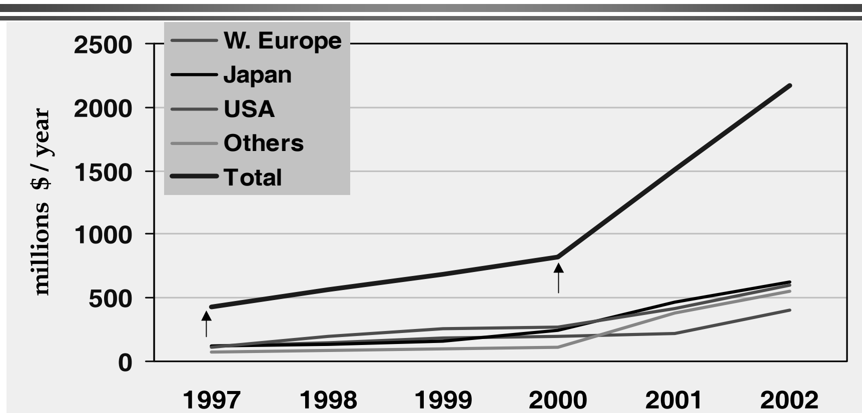
Nanotechnology in the World

(est. $1 Trillion revenue worldwide by 2015!)



NNI: 27% of world nanotech investment

NNI: 0.6% of U.S. Federal R&D

Senate Briefing, May 24, 2001 (M.C. Roco), updated on April 30, 2002

NNI: R&D Funding by Agency

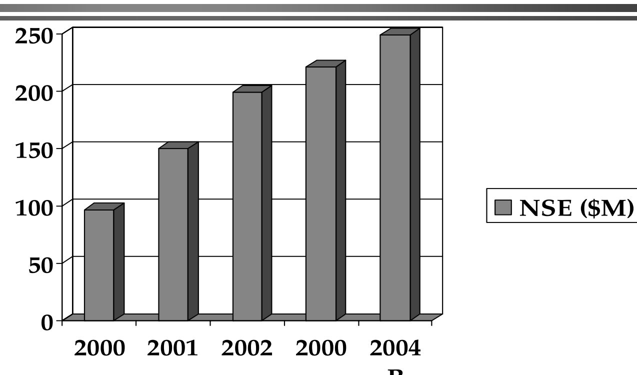
Fiscal year (all in million $)	2000	2001 Enacted/actual	2002 Enacted/actual	2003	2004 Request
National Science Foundation	97	150 /150	199 /204	221	249
Department of Defense	70	110 /125	180 /224	243	222
Department of Energy	58	93 /88	91.1 /89	133	197
National Institutes of Health	32	39 /39.6	40.8 /59	65	70
NASA	5	20 /22/	35 /35	33	31
NIST	8	10 /33.4	37.6 /77	66	62
Environmental Protection Agency	-	/5.8	5 /6	5	5
Homeland Security (TSA)	-		2 /2	2	2
Department of Agriculture	-	/1.5	1.5 /0	1	10
Department of Justice	-	/1.4	1.4 /1	1.4	1.4
TOTAL	270.0	422.0 /464.7	~ 600 /697	~ 770	~ 849

Other NNI (NSET) participants:
OSTP, NSTC, OMB, DOC, DOS, DOT, DOTreas, FDA, NRC, DHS, IC

M.C. Roco, NSF, 8/21/03

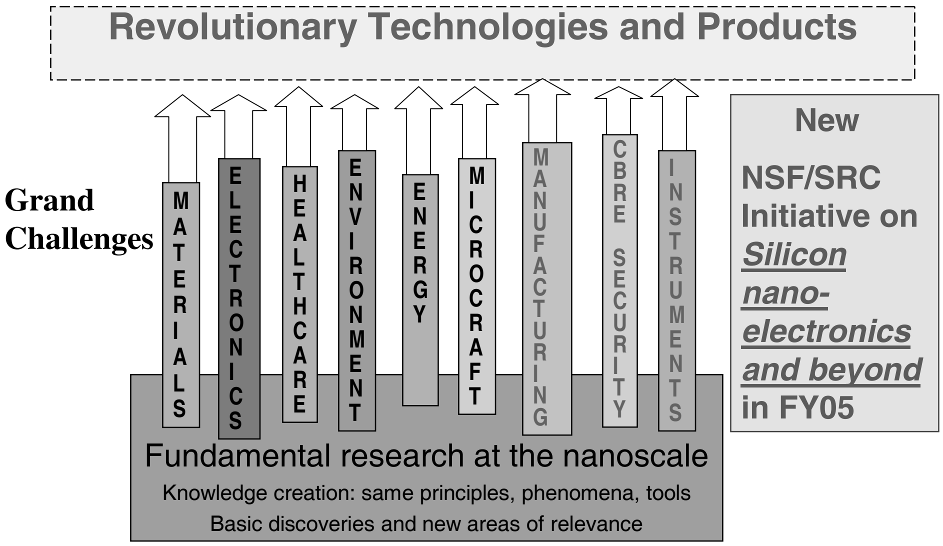
NSF Nano Science & Enginnering (NSE)

Trend expected to continue !



- **Nanostructure 'by Design', Novel Phenomena** 45%
  physical, biological, electronic, optical, magnetic
- **Device and System Architecture** 20%
  interconnect, system integration, pathways

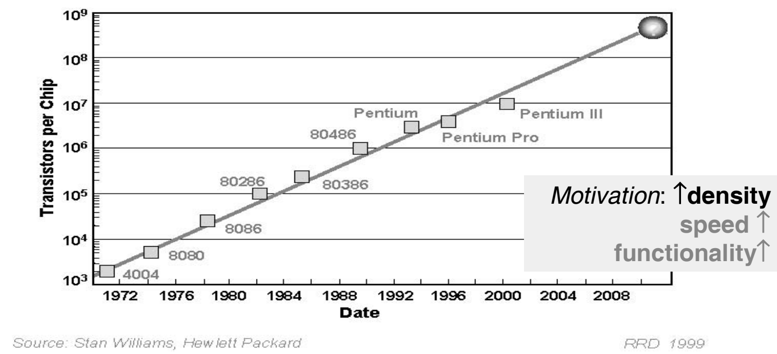
"Horizontal" knowledge creation
"Vertical" transition to Grand Challenges



NSE Program Details

1. **Nanoscale Interdisciplinary Research Teams (NIRT):** approx. 70 large awards/yr
2. **Nanoscale Exploratory Research (NER):** 80 awards/yr
3. **Nanoscale Science & Engineering Centers (NSEC):** 8 centers so far
4. **Nanoscale Science & Engineering Education (NSEE):** 35 awards/yr
5. **National Nanotechnology Infrastructure Network (NNIN):** initial stages

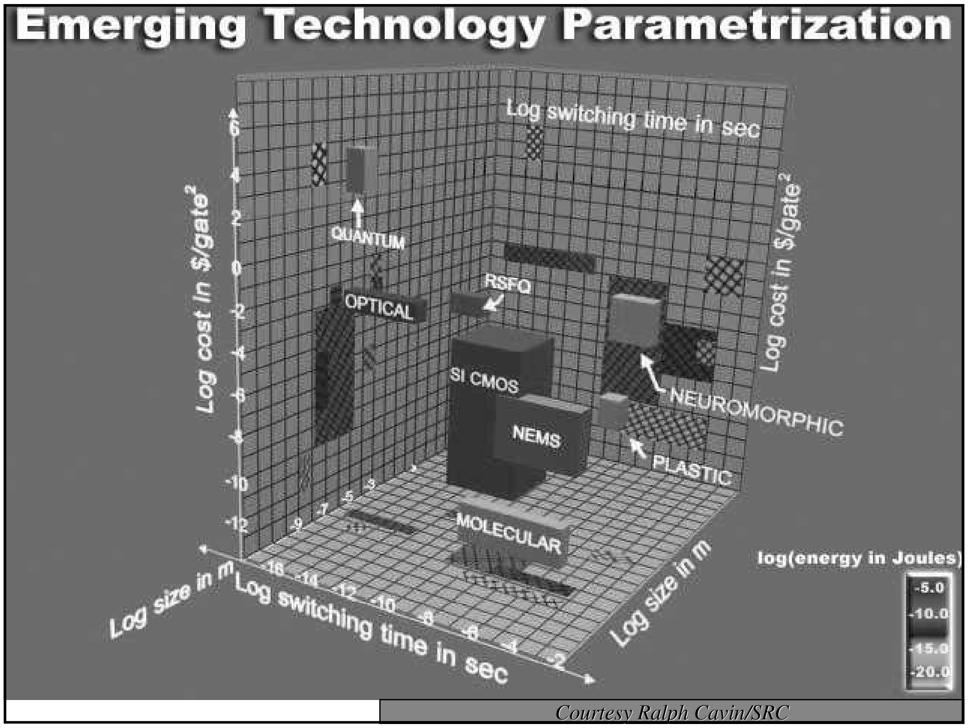
Moore's Law: Transistors per chip



Responsible for major productivity gain during the last decade

Conventional vs Nanocomputing Projections

- Conventional CMOS scaling will continue for the next 10-15 years
- Heterogeneous new technologies will begin to be integrated into Si platforms by 2015
- Novel nanotech devices needed beyond 2015.
- Considerable lead time needed
- Compatability with CMOS will leverage existing learning and enable compatibility earlier production of non earlier production of non-CMOS nanodevices



Basic Nano-Building Blocks

- Carbon nano-tubes (CNT) as transistors, inteconnects
- Single Electron Transistors (SET)
- Non-charge based devices (spin/photonic devices)
- Quantum dots & QCAs
- Molecular devices and eventually architectures
- Still others, FinFETs, RTDs, crossbars ….

Basic Nano-Building Blocks

Issues arise at each level:

- Devices (1 device)
- Circuits (10 devices)
- Blocks (1k devices)
- Systems (10k-1M devices)
- Architechtures (1M – 1B devices)

- Power/heat removal is more of a concern in "smaller" devices: reversible computing? non-charge transfer devices? Clock slow-down, use parallelism? micro-fluidic cooling?

Nano-issues in computing

- Techniques for design of reliable systems constructed from unreliable and imprecise components.
- Are there fault models adequate at the nano-scale?
- Are there designed-in self-testing techniques at the nano-scale?
- Are the current generation of design tools applicable at the nano-scale? If not, what needs to be developed?
- Architectures may need to be non-vonNeuman (CNN like?), may exploit asynchronous computing, reconfigurable, defect tolerant ….
- Self-assembly (chemical, biological) may have to be envisaged

Nano-issues in computing (cont'd)

- Can electron spin (spin-tronics) be of use?
- Scalability of new technologies?
- Separation of the design process from the underlying medium?
- Models of computation, abstraction and design hierarchies. Possible carry over from silicon VLSI:
    - Architecture => Layout => Timing model

Nanocomputing-What to do?

- Promote dialogue between the silicon design community and non-silicon technologists
- Joint SRC/NSF workshops in areas:
    - Logic
    - Memory
    - Architecture
- Joint SRC/NSF solicitation in Oct, '04 on "Silicon Nanoelectronics and Beyond (SNB)"

Thank you